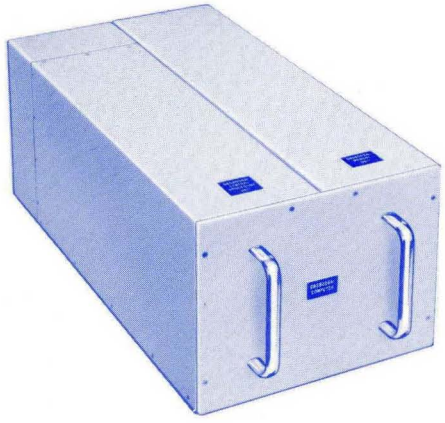
11/65



ALERT

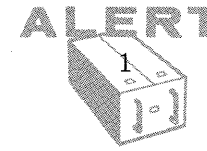
GENERAL PURPOSE DIGITAL COMPUTER

Honeywell *Military Products Group* AERONAUTICAL DIVISION — ST. PETERSBURG, FLORIDA

CONTENTS

Honeywell introduces the *ALERT*, newest in its line of general-purpose digital computers. *ALERT* is an extremely fast, versatile, compact, rugged, multi-application computer. By outlining Honeywell's approach to computer design, an easy comparison can be made to other present-day machines. The reader will readily grasp the computer's advantages for his particular application as operation is described.

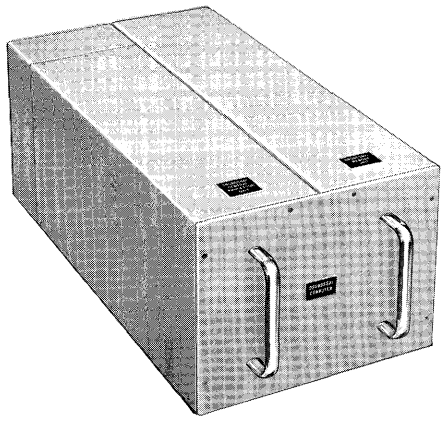
ALERT meets the requirements for most scientific computer needs. Expandable memory and flexible input/output design allows logic, data moving and binary arithmetic operations at speeds suitable for both airborne and ground-based applications. Rigorous environmental packaging is also compact enough for installations in manned aircraft, missiles or any vehicle operating in adverse conditions with limited equipment space. The instruction repertoire has been optimized to provide more effective hardware utilization, yet adequate for efficient handling of complex equations. An ample software package has been developed with the user in mind. *ALERT* is a complete computer: versatile, maintainable, reliable.



ALERT IN BRIEF

Before describing *ALERT* in detail, its general characteristics are summarized to illustrate features beyond those of the average general-purpose computer. The summary includes *ALERT* features interwoven with items necessary in all general-purpose computers so that a fair comparison can be made to other similar machines.

THE BASIC COMPUTER



ALERT, in its basic configuration, consists of two separate modules interconnected to form one off-the-shelf general-purpose scientific computer.

The basic computer combines a central processor with a memory module having a word capacity chosen to fit individual needs. This combination offers:

- Parallel organization - single address operation.
- 24-bit word length.
- Six index registers.
- Indirect addressing.
- Priority interrupt externally.
- Character handling.
- Completely solid-state construction using:

  Integrated circuitry in 14 and 40 lead flatpacks.

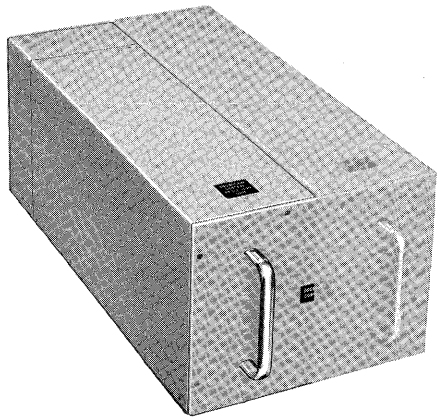
  Microbiax memory (core memory available).
- 10, 000-hour MTBF.
- Options of:

  Input/output expansion.

  Priority interrupt expansion to 24 levels.

  Memory expansion from 4, 096 to 32, 768 24-bit words.

CENTRAL PROCESSOR



ALERT central processor is 5 inches by 7.6 inches by 19.5 inches and contains a direct input/output channel in addition to circuitry necessary to perform arithmetic functions. Characteristics include:

- High speed executions (compared with leading commercial scientific machine):

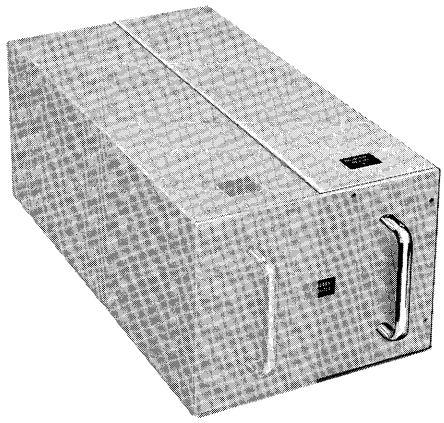
	IBM 7090	*ALERT*
ADD	4.4 μsec	2.0 μsec
SUBTRACT	4.4 μsec	2.0 μsec
MULTIPLY	25.3 μsec	12.0 μsec
DIVIDE	30.5 μsec	30.0 μsec

- Divide overcapacity check.
- Overflow check.

Eight HLTTL integrated circuit configurations feature:

- 14 and 40-lead flatpack construction.
- Low power consumption.
- High speed operation.
- High noise immunity.
- High capacitance-driving ability.
- High fan-out capability.

MEMORY



Memory modules vary in size according to number of words. The basic 4,096 word module is 5 inches by 7.6 inches by 19.5 inches and the fully expanded 32,768 word version increases width to 25.25 inches. Height and depth remain constant. Characteristics include:

- Microbiax memory elements.
- Nondestructive readout.
- High speed operation of:

  1 microsecond - read

  4 microseconds - write.
- Self-contained solid-state memory electronics using monolithic integrated and thin-film circuits.
- No discrete diodes in memory stack.

In addition, a DRO core memory configuration is available. Characteristics include:

- Magnetic cores.
- High speed operation of:

  1-4 microseconds read-write.

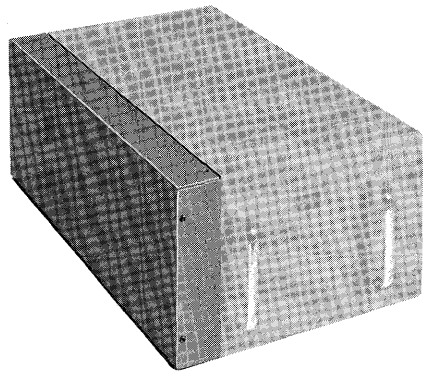
- Hybrid components:

  Integrated circuitry

  Discrete components.

This configuration is also expandable to 32, 768 words.

BUFFERED INPUT/OUTPUT CHANNEL



Flexibility is gained by adding a buffered input / output channel to the basic configuration. Contained in a plug-in module 2.5 inches by 7.6 inches by 19.5 inches, the buffered channel allows *ALERT* to communicate with magnetic tape devices, line printers, card readers, card punch input devices and drum units. With this addition, *ALERT* is expanded to include:

- Up to three read-write channels.
- Up to eight peripheral control units.
- Up to eight high speed devices per peripheral control unit.
- Maximum capacity of 64 high speed devices.
- Input and output transfer rates of up to 6.0 microseconds.

GENERAL CHARACTERISTICS

ALERT complies with MIL-E-5400 and is designed to meet the requirements of MIL-I-26600 (RFI). Mean-time-between-failure design goal is 10,000 hours.

Physical characteristics are tabulated on the following page. Included are the buffered input/output and central processor weight, power and volume together with various memory configuration statistics.

MEMORY

CAPACITY	4K	6K	8K	12K	16K
SIZE (FT^3)	0.43	0.57	0.57	0.73	0.94
WEIGHT (LBS)	20	27	31	44	57
POWER (WATTS)*	54	64	74	84	94

* AT 25°C AND 25% WRITE (ALL READ-WRITE MEMORY)

CENTRAL PROCESSOR	BUFFERED INPUT/OUTPUT
0.43 FT^3	0.21 FT^3
19 LBS.	10 LBS.
60 WATTS	60 WATTS

A complete software package is available including:

Program Loader	Dump Routine
Scientific Subroutines	Diagnostics
Source Program Update	Simulator
Assembly Systems	Executive Program
Input/Output	Options.

The following pages describe *ALERT* operation, packaging, programming, and accessories. Applications will be evident and Honeywell invites requests for additional information concerning the newest approach to general-purpose digital scientific computing techniques.

TECHNICAL DESCRIPTION

BACKGROUND

ALERT is the culmination of a carefully planned development program at Honeywell. The program produced not only the fast, multiapplication *ALERT* computer, but a firm technology base for a diversified family of machines. Advances incorporated in this machine may readily be carried over into designs ranging from sophisticated multiprocessors to austere serial or modified parallel processors. Packaging and circuitry may be applied directly; logical organization requires straightforward extensions of *ALERT* techniques.

Basis for *ALERT* development was derived from previous Honeywell airborne computer projects. Various circuits and memory configurations were used in planned evolution to arrive at the best combination to produce a fast, compact, versatile scientific computer suitable for many applications. The steps to circuit and memory selection are illustrated in Figure 1.

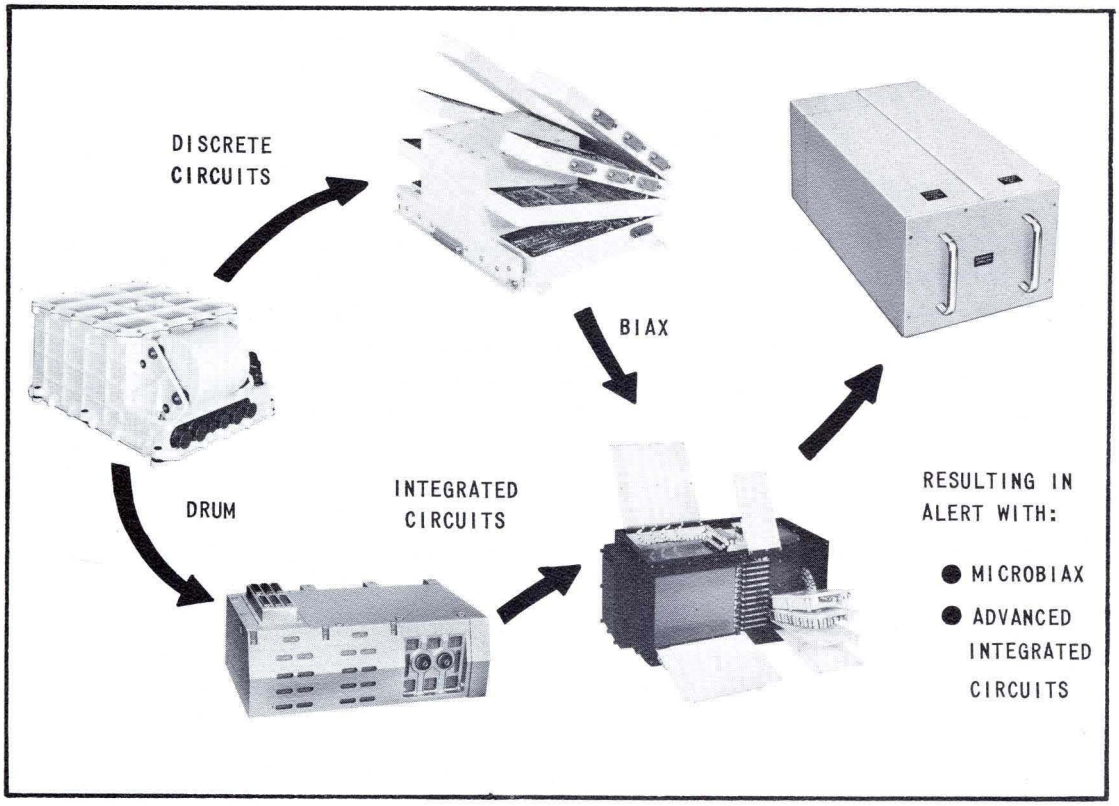
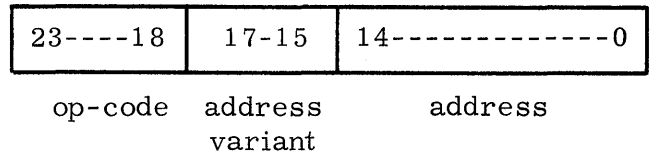


FIGURE 1. COMBINATIONS OF CIRCUITRY AND MEMORIES LEADING TO ALERT.

From the drum memory, discrete circuit concept two machines were developed. The better features of these machines were combined to form a foundation for *ALERT*. State of the art advances in both circuitry and memory elements were then incorporated. Combined with efficient logic design, optimum use of multilayer printed circuitry, and packaging techniques with reliability, environmental ruggedness, and maintenance the key considerations, the development goal was achieved. The following pages describe *ALERT* technical aspects in detail.

WORD FORMAT

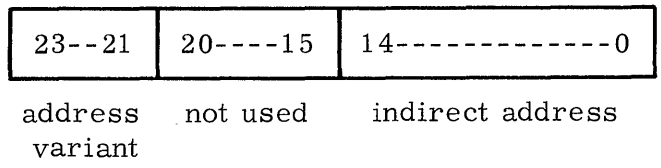
ALERT uses a 24-bit word for both instructions and data. The instruction word is in three segments: op-code, address variant, and address.



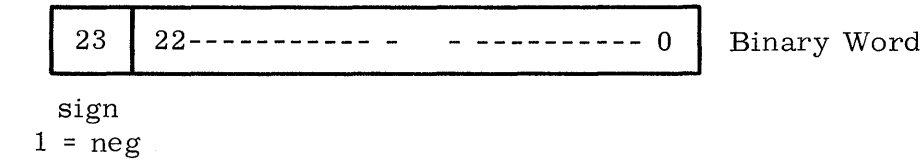
Each instruction is identified by the six high-order bits comprising the op-code (providing up to 64 instructions). In some cases, the op-code identifies a category of instructions and the address variant distinguishes between instructions within the category (see NAD in Instruction List, Programming section). In general, the address variant is used to specify an instruction as direct, indirect or indexed. The variant codes are:

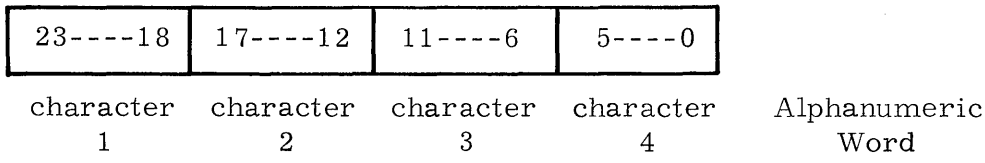
000	Direct Address	100	Index Register No. 4
001	Index Register No. 1	101	Index Register No. 5
010	Index Register No. 2	110	Index Register No. 6
011	Index Register No. 3	111	Indirect Address.

The word location in memory is specified by the 15 low-order bits of the instruction word permitting continuous addressing of up to 32,768 words. If the address variant specifies an indirect address, the memory location of the indirect address word is contained in the address segment of the instruction word. The indirect address word format contains only address variant and indirect address. The computer may be indirect addressed, as many times in succession as required.



Data words are in two forms, either binary or alphanumeric. The binary word contains 23 information bits plus sign. This word is broken into segments to represent the alphanumeric word.





INSTRUCTIONS

A detailed instruction list is presented in the programming section on page 56. For logic and operation discussion the following list has been summarized and grouped by function. The summary includes mnemonic, definition, and execution time.

CONTROL		
BAR	- Branch and return	6 μsec.
EXC	- Execute	1 μsec.
HLT	- Halt	2 + Δμsec.
JAN	- Jump on accumulator negative	2 μsec.
JAP	- Jump on accumulator positive	2 μsec.
JAZ	- Jump on accumulator zero	2 μsec.
JMP	- Jump	2 μsec.
PAS	- Pass	2 μsec.
SKM	- Skip if accumulator and memory are equal	4 μsec.
SKN	- Skip if signal is not set	3 μsec.
SMZ	- Skip if memory is zero	3 μsec.
FIXED POINT		
ADD	- Add to accumulator	2 μsec.
ADM	- Add to memory	7 μsec.
DIV	- Divide	30 μsec.
MPY	- Multiply	12 μsec.
SUB	- Subtract from accumulator	2 μsec.
TLY	- Tally	7 μsec.
DIRECT INPUT/OUTPUT		
PIN	- Peripheral input	8 μsec. if SKIP 4 μsec. if NO SKIP
POT	- Peripheral output	4 μsec.
SKC	- Control and skip	4 μsec.
STE	- Set external point	2 μsec.
SKE	- Skip if external signal is not set	3 μsec
LOGIC		
EXT	- Extract (logical AND)	2 μsec.
HAD	- Half add (exclusive OR)	2 μsec.
SMP	- Superimposed (inclusive OR)	2 μsec.
SST	- Substitute	7 μsec.

BUFFERED INPUT/OUTPUT

PCB	- Peripheral control and branch	$3 + \frac{29C}{4}$ μsec.
PDT	- Peripheral data transfer	$3 + \frac{33C}{4}$ μsec.

INTERRUPT

LIM	- Load interrupt mask	2 μsec.
SRB	- Set/reset interrupt block	2 μsec.
STI	- Store interrupt register	6 μsec.
XML	- Exchange interrupt mask	6 μsec.

INDEXING

AIX	- Augment index immediate	2 μsec.
DJX	- Decrement and jump on index not zero	2 μsec.
JIX	- Jump on index not zero	2 μsec.
STX	- Store index register	6 μsec.
SXI	- Skip immediate on index high	3 μsec.
AUX	- Augment index	3 μsec.
LDX	- Low index register	2 μsec.
SKX	- Skip on index high	4 μsec.

WORD TRANSMISSION

ALR	- Alter register	2 μsec.

(See V = 2, NAD instruction in Programming Section)

DLD	- Double-precision load	3 μsec.
DST	- Double-precision store	10 μsec.
LDA	- Load accumulator	2 μsec.
LDB	- Load B register	2 μsec.
RSS	- Restore status	2 μsec.
STA	- Store accumulator	6 μsec.
STB	- Store B register	6 μsec.
STS	- Store status	7 μsec.

CHARACTER

CSK	- Characters skip if equal	5 μsec.
LCH	- Load character	2 μsec.
SCH	- Store character	7 μsec.

SHIFT

SFT	- Shift	2 + nμsec.

(See V = 1, NAD instruction in Programming Section)

ADDRESSING LOGIC

ALERT addressing is performed by logic circuitry within the blocks emphasized on the diagram. The function of each block is described. Reference will be made to instructions used for addressing. A summary list is included in this section and a more detailed list is presented in the programming section.

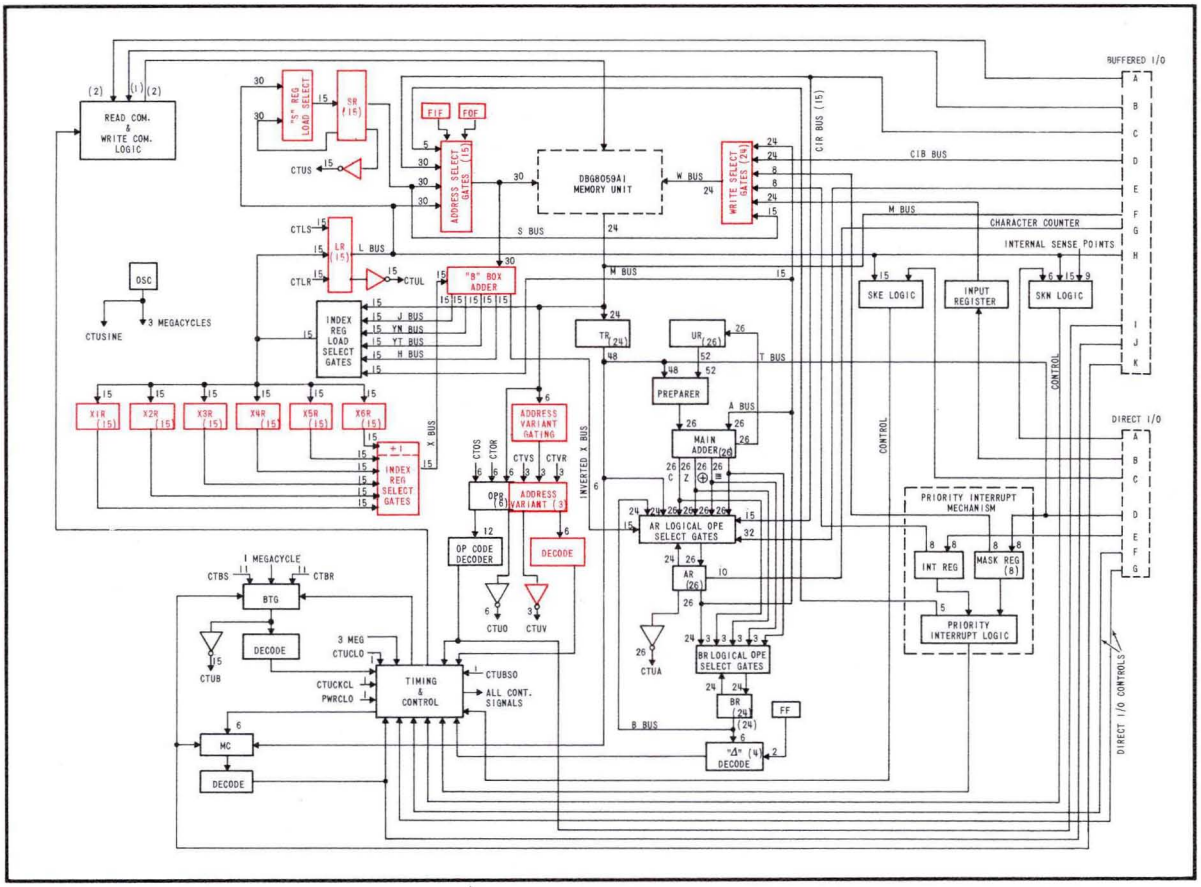


FIGURE 2. ADDRESSING LOGIC EMPHASIZED IN CENTRAL PROCESSOR.

PROGRAM COUNTER (SR) - holds the instruction address and sequences the execution of the stored program. Containing 15 bits, it is capable of addressing 32,768 memory words. The BAR order stores the contents of the program counter in memory.

OPERAND ADDRESS REGISTER (LR) - normally holds the 15-bit operand memory address. It can address 32,768 operands in memory. When instructed by the AIX order, it becomes the augment of the specified index register. The operand address register is normally loaded from memory through the index register load select gates. In some cases, its bits are used for further instruction decoding for "no address" instructions.

SR LOAD SELECT - provides logic for transferring the contents of the LR into the SR when instructed by jump orders. It also operates as counter logic for the SR.

ADDRESS SELECT GATES - are used to connect the appropriate address to memory from either the buffered input/output, interrupt logic, program counter, or operand address register. The operand address is connected to the B box adder through these gates for adding the operand address to the contents of specified index registers. When instructed by the DJX order, a minus one is forced in the B box adder to effectively decrement the index register by one.

INDEX REGISTER LOAD SELECT GATES - are used to load the operand address register from memory. A specified index register may also be loaded through these gates from the B box adder, memory, or the A register.

INDEX REGISTERS (X1R - X6R) - are six 15-bit registers which provide effective operand address of program control (such as countdown). These registers are loaded by the index register load select gates. The select gates connect the index registers to the B box adder. Since the index registers are not binary counters, countdown is performed through the B box adder.

INDEX REGISTER SELECT GATES - are used to connect one of six index registers to the B box adder. The gates also transfer specified index registers to the A register.

B BOX ADDER - contains a 15-bit capacity. It is used to increment either a specified index register or the operand register. Addition is performed in one microsecond.

ADDRESS VARIANT GATING, REGISTER, DECODE - are illustrated on the diagram as three separate blocks. Upon instruction fetch, the address variant gating logic connects bits 16 through 18 to the variant register. These bits are then decoded by the address variant decode logic. An indirect address causes bits 22 through 24 to be gated into the address variant register.

WRITE SELECT GATES - connect one of six sources to the memory for writing. These sources are the program counter, A register, mask register, interrupt register, direct I/O input register, and the buffered I/O.

CTU DISPLAY DRIVERS - are provided to monitor the addressing logic during operation.

TIMING AND CONTROL LOGIC

The blocks emphasized on the diagram comprise *ALERT* timing and control logic. Most computer operations depend on this group of logic for proper execution. Functions of each block are described briefly.

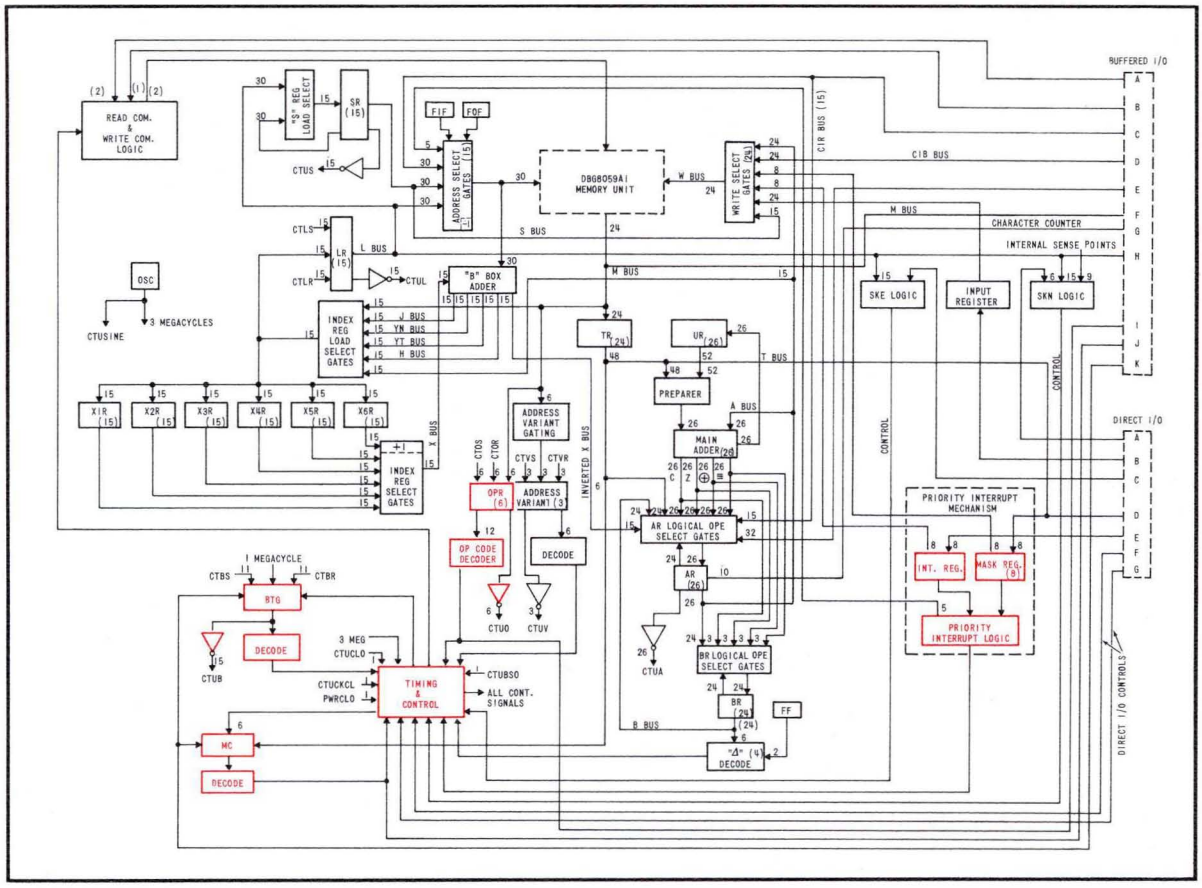


FIGURE 3. TIMING AND CONTROL LOGIC EMPHASIZED IN CENTRAL PROCESSOR.

MACRO COUNTER (MC) - is a 6-bit macro counter that counts iterations in the larger instructions such as multiply, divide and the shift orders. The N count of a shift operation is loaded from the macro counter from the T register. In either multiply or divide, the macro counter is preset to the number of iterations to be executed in the order.

OP CODE REGISTER (OPR) - holds the 6-bit operation code. It is loaded from memory M bus. It provides the basic control for the computer.

OP CODE DECODER - decodes the 6-bit op-code into specific commands.

MACRO COUNTER DECODE - decodes the counts from the macro counter.

BIT TIME GENERATOR (BTG) provides the basic timing for execution of all orders. It is a selectively advanced 11-bit ring counter.

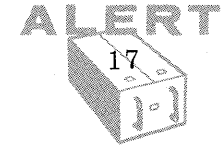
BIT TIME GENERATOR DECODE - decodes the specific bit times needed to execute instructions.

TIMING AND CONTROL LOGIC - provides the various subcommands for the central processor, whereas the other blocks being described are timing and control for the entire computer. An example of its operation is generation of basic controls, such as ATB, which initiates transfer of A register contents into the B register.

INTERRUPT MASK REGISTER (FSK) - blocks all or selected interrupts set in the interrupt register. It provides programmer control for external interrupts. This is an eight-bit register in the basic system, but is expandable to 24 bits. The interrupt mask register is loaded by program through the T register.

PRIORITY INTERRUPT LOGIC - connects, by priority, the external interrupts to the central processor.

CTU DISPLAY DRIVERS - allow the bit time generator, phase generator, and other minor functions to be monitored during operation.



ARITHMETIC LOGIC

Arithmetic functions are performed by the logic contained in the blocks emphasized on the diagram. Each function will be described briefly.

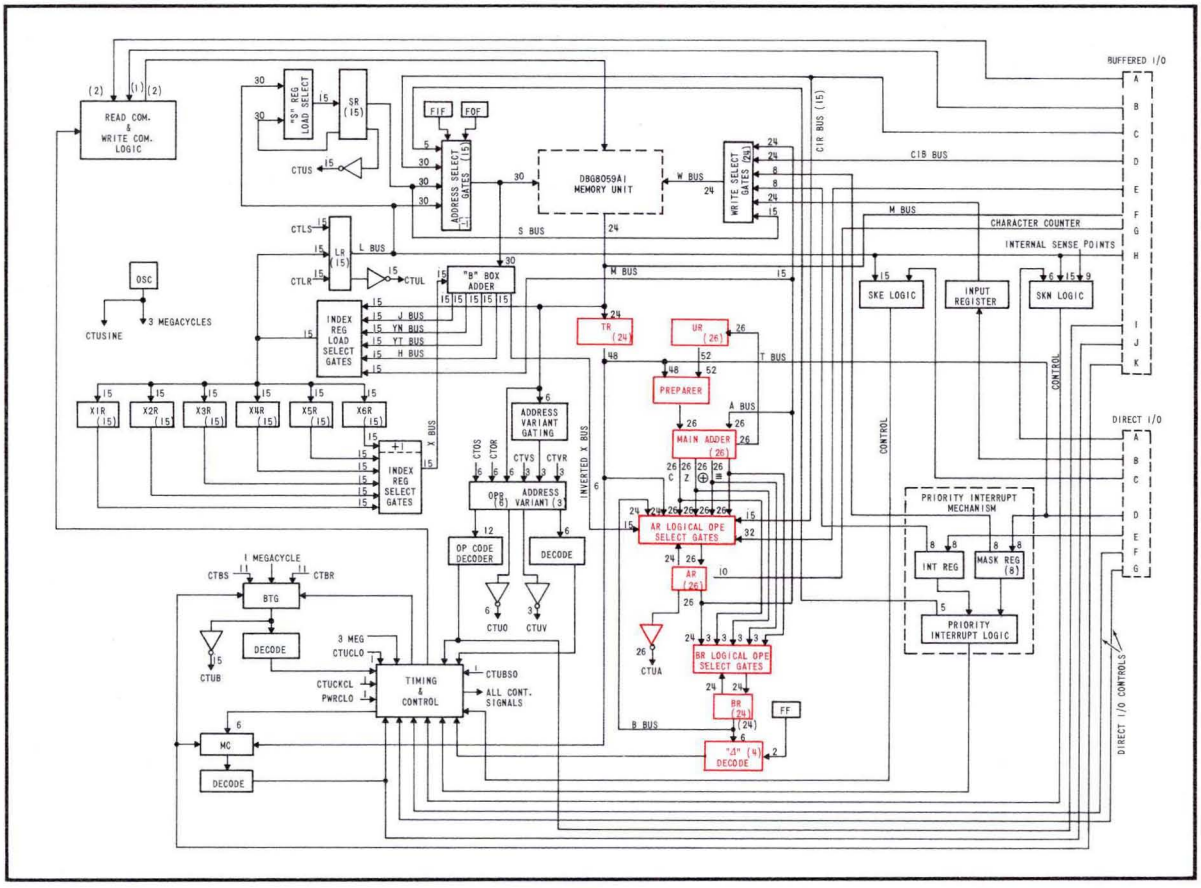


FIGURE 4. ARITHMETIC LOGIC EMPHASIZED IN CENTRAL PROCESSOR.

BR LOGICAL OPERATION SELECT GATES - perform the following gating into the B register:

- Transfer A register into B register.
- Provide means for shifting right and left.
- Three-bit right shift for multiply delta generation with three low-order bits of A register to three high order bits to B register.
- One-bit left shift for divide generation of quotient.

PREPARER - is essentially a 26-bit shift matrix. It connects the various complemented or uncomplemented multiples of the T register. It also connects the U register to the main adder.

MAIN ADDER - contains 26 bits and performs all additions and subtractions in the computer. It adds the contents of the T or U register to the A register contents. The results are then placed in the A register. The adder is parallel and is comprised of six carry-predict networks.

AR LOGICAL OPERATION SELECT GATES - provide gating to load the A register for the following functions:

- Transfer adder result to A register.
- Transfer B register to A register.
- Transfer contents of specified index register to A register.
- Transfer contents of T register to A register.
- Transfer C1R register of buffered I/O to A register.
- Perform ring sum of T and A register, placing results in A register.
- Perform inclusive OR of A register in T register with results in A register.
- Superimpose memory content and B register with results in A register.
- Provide means for shifting right or left.

A REGISTER (AR) - contributes one operand to arithmetic and logical operations and holds results of these operations unless instructed otherwise. This 26-bit register holds the high-order product of a multiplication or the quotient of a divide. The A register also serves as the status register during the write operation of an operand (Upper Accumulator).

TRANSFER REGISTER (TR) - is loaded from memory and used as one of the operand registers during arithmetic orders. A POT order causes this 24-bit register to hold information that is placed on the output bus.

THREE TIMES ICAND REGISTER (UR) - contains 26 bits and is used to hold the multiplicand during the multiply operation. On certain orders, it is used to manipulate words in the A register. This register is not available to programmers.

DELTA DECODE (Δ) - decodes the effective three-bit bite multiplier in multiplication.

B REGISTER (BR) - is a 24-bit lower accumulator. It holds the multiplier at the beginning of a multiply operation and the lower order product at the end of a multiply instruction. During divide, it generates the quotient, bit by bit, and holds the final remainder. The B register is used as the low-order 24 bits of a double precision word.

CTU DISPLAY DRIVERS - allow the A register to be monitored by the CTU.

INPUT/OUTPUT FACILITIES

Information in and out of *ALERT* may be routed through either the direct input/output channel located in the central processor or the buffered input/output unit. If the buffered channel is not used, its plug may be used for additional inputs also. A description of the two devices follows.

DIRECT INPUT/OUTPUT CHANNEL

The direct input/output channel provides an interface between the *ALERT* central processor and external devices. Emphasized on the block diagram are the functional blocks used during input/output operations. A brief description of methods used to communicate with external devices will be given, rather than describing each block involved. Functions will be evident after the methods are discussed.

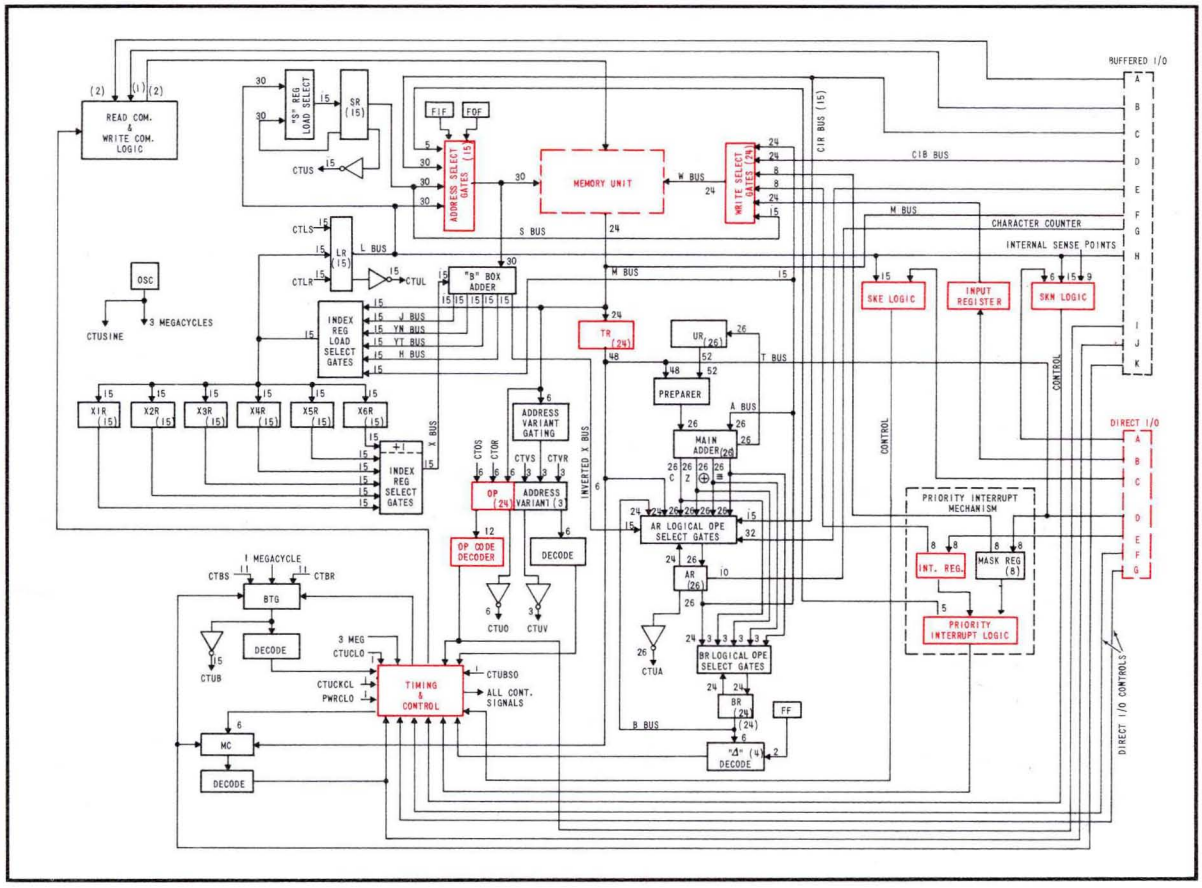


FIGURE 5. DIRECT INPUT/OUTPUT SCHEME IN CENTRAL PROCESSOR.

The *ALERT* can communicate with three classes of external devices characterized as:

- Those only requiring outputs from the computer.
- Those only providing inputs to the computer.
- Those which exhibit both input and output properties.

Examples of each class are:

- Output - Paper tape punches, printer, D/A converters, gyro torquers, stepper motors, displays, and registers.
- Input - Paper tape readers, typewriters, A/D converters, ΔV precounters, encoders, and register.

The direct input/output channel is under program control for all operations. Six instructions are used to communicate with external devices. This group of orders is used to interrogate, select, and control the device during transaction, and command data transfer into and out of the central processor. The orders, by category, are:

- Input Discretes:

  SKN - Skip if internal signal is not set.

  SKE - Skip if external signal is not set.

- Output Discrete:

  STE - Set external point.

- Selection and interrogation or control:

  SKC - Control and skip

- Data Transfer:

  POT - Peripheral output and skip.

  PIN - Peripheral input and skip.

  (See programming section for detailed description.)

To illustrate the use of these orders in actual operation, each class of external device will be discussed in a general situation.

Input Devices

All input devices share a common input bus and are selected for connection to this bus by execution of the SKC order. This order may either issue inquiries to the device or command it to perform certain functions. An example of SKC use is:

- Address device number five.
- Question the device's readiness to transact.
- Command device to rewind tape.

Fifteen bits are available to address and control external devices, and these bits may be employed in any combination of control and address desired. For example, one popular combination is to use the nine low-order bits for addressing and the six high-order bits for control. Upon execution of an SKC order, an SKC strobe is generated and used to ask the external device selected if it is ready. The device must acknowledge this request within the strobe time, to be accepted by the processor. Upon acceptance, the processor generates a response/acknowledge signal which is sent to the selected external device. This two-way communication between central processor and external device insures that both units are ready for information transfer. If the external device addressed by the SKC order is busy, it will not generate a response within the SKC strobe time. When this happens the program counter is advanced an additional step as shown in Figure 6.

For data transfer, a PIN order is executed. This order is usually preceded by an SKC order to select the desired external device and ascertain its readiness to transact. The PIN order causes another strobe signal to be generated, and the same recognition sequence performed in the SKC order is repeated. Upon completion of recognition, the information to be transferred is clocked into the input register and recorded in memory in parallel. The procedure and rate for maximum input transfer is illustrated in Figure 6. The external device selected by an SKC order remains connected to the input bus until the next SKC order is executed.

Program branch decisions are based on external or internal conditions sensed by discrete signals at points tested by the SKE and SKN orders. The SKE order is used to sense external discretes, and the SKN order, internal discretes. During these orders the point to be sensed is divided by a one in a specified bit position in the address field. Six of the internal discretes are located in the Computer Test Unit (CTU). When the

CTU is not connected to the system (when the equipment is airborne), SKN may be used to sense an additional six external signals by connecting to the plug normally used for the CTU connection.

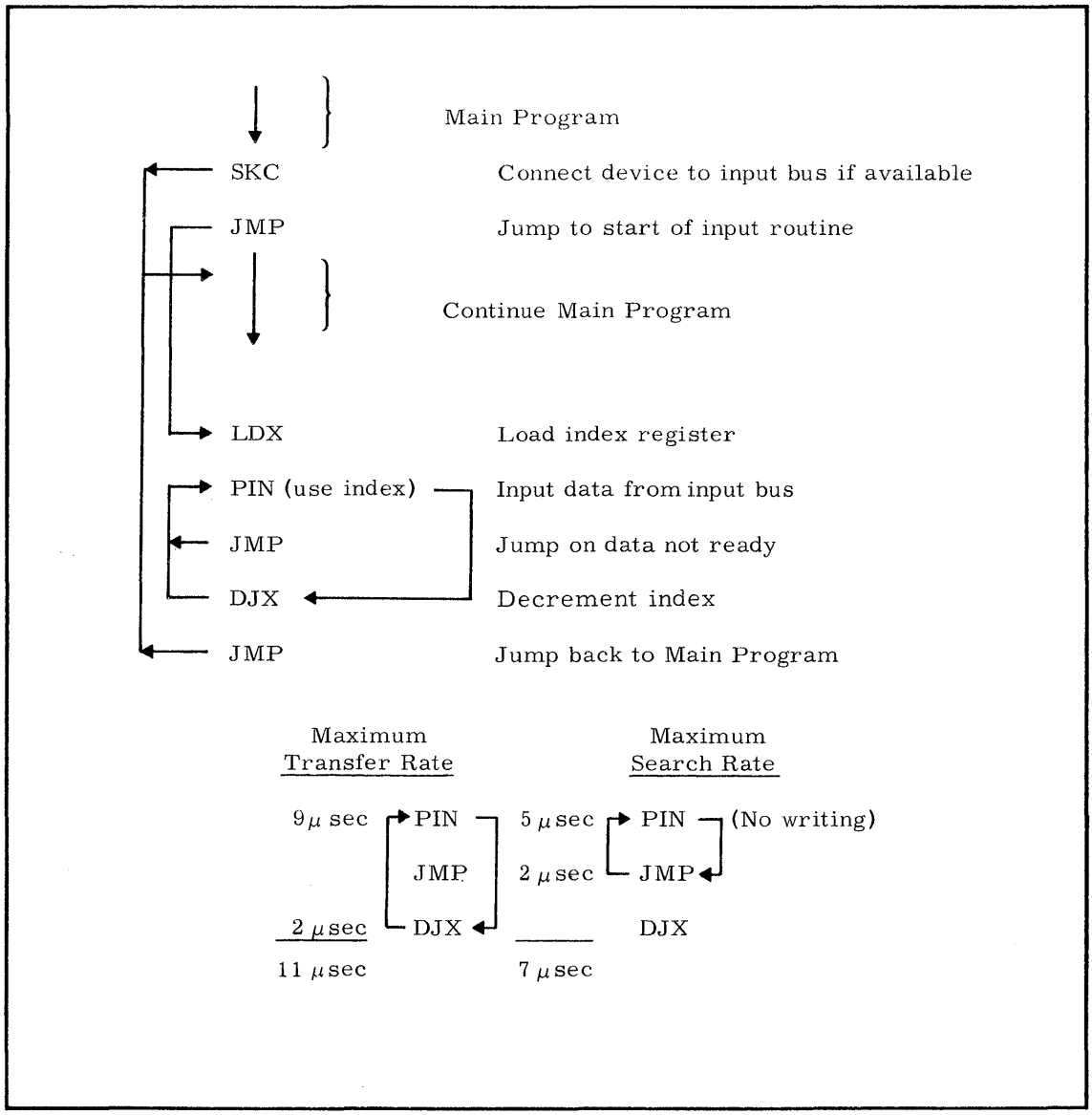


FIGURE 6. PROCEDURE AND RATE FOR MAXIMUM INPUT TRANSFER.

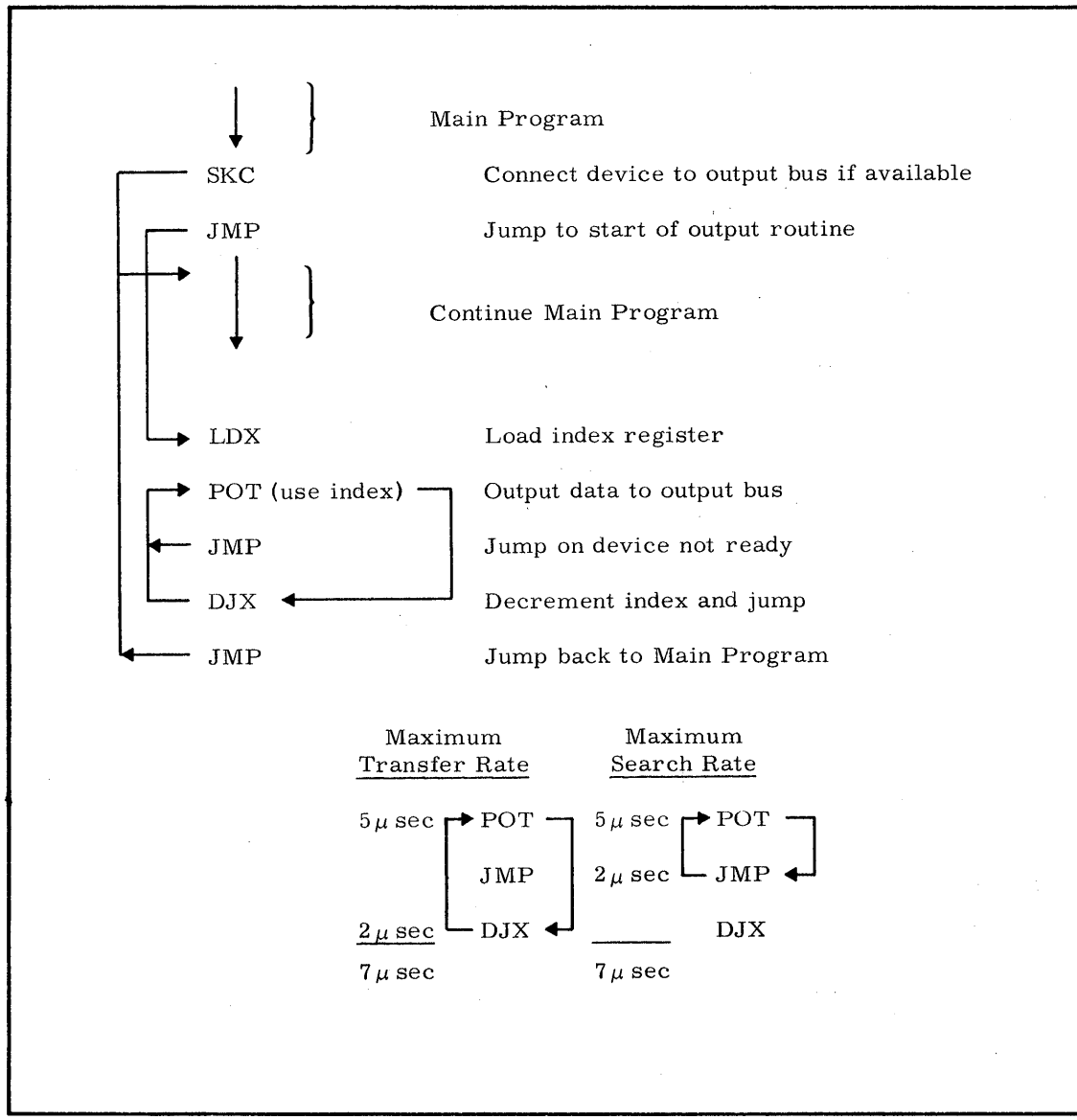


FIGURE 7. PROCEDURE AND RATE FOR MAXIMUM OUTPUT TRANSFER.

Output Devices

A common bus services all direct output devices. When more than one external device is connected, selection and control of the transaction is by execution of the SKC order. The SKC execution is identical to the sequence used for input devices.

Data transfer is transacted by executing the POT order. The same steps are used to transfer data in parallel out of *ALERT* as were described for input transfer. An SKC is issued to select the device, recognition action takes place, the POT order is given and the POT strobe causes the external device to acknowledge that transfer had occurred. Maximum output transfer rate and procedure is illustrated in Figure 7.

Discrete outputs may be generated by executing a STE order. A particular external point is selected by bit position in the address field and a one microsecond pulse is sent to the selected point. Fifteen external points can be serviced without external decoding. With decoding, as many as 32, 768 points may be serviced.

Input/Output Devices

This class of peripheral equipment may use all six orders for transactions with the central processor. These external devices are treated as either input or output peripherals and transactions are as previously described. When an input/output device is to be communicated with for both input and output transactions in succession, the first transaction is completed then the device is addressed again for the second as if it were another peripheral.

BUFFERED INPUT/OUTPUT CHANNEL

The buffered input/output channel consisting of one read-write channel (RWC) is a separate module that contains logic and circuitry for outside communication with the *ALERT* main memory. In conjunction with external peripheral control units, the buffered input/output channel with one RWC can time-share between as many as 64 peripheral units. With three read-write channels, 3 of the 64 peripheral units can communicate with the central processor simultaneously. The initiation of communication is under program control, using the Peripheral Control and Branch (PCB) and Peripheral Data Transfer (PDT) orders listed in the instruction list. Further action of the buffered input/output channel is asynchronous with the central processor.

The basic diagram in Figure 8 illustrates information flow between the peripheral devices and the central processor main memory. One read-write channel is shown connected to Peripheral Control Units (PCU) one through eight. Each PCU can service up to eight devices, such as line printers, magnetic tape units, card readers, and tape readers. The function of the buffered input/output channel is to control and keep status on the communications.

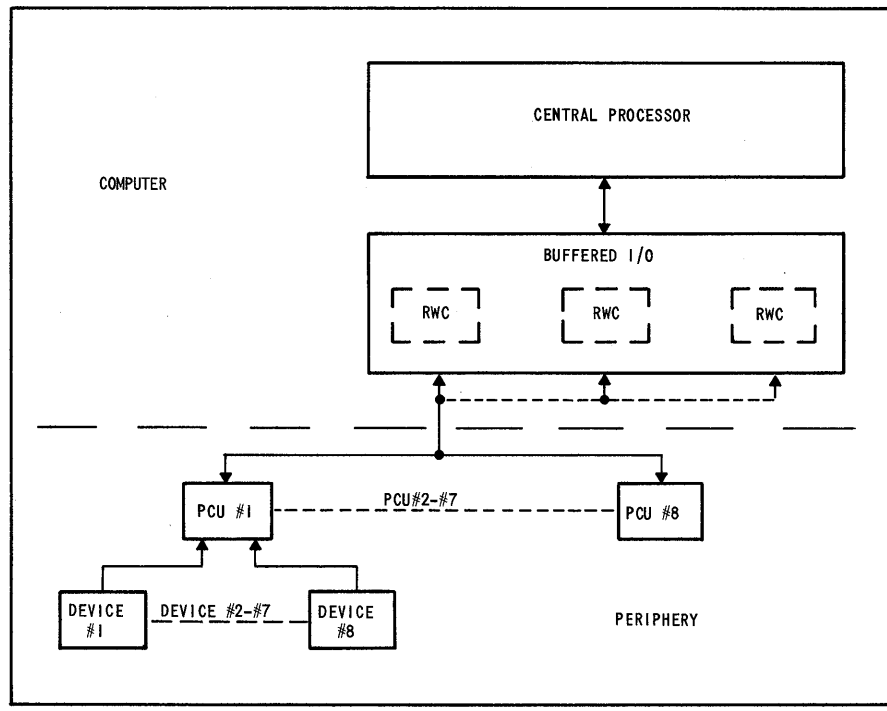


FIGURE 8. INFORMATION FLOW BETWEEN PERIPHERAL DEVICES AND ALERT.

To illustrate the communication procedure between main memory and external devices, a sample interrogation is given. Execution of a PCB instruction generally precedes a PDT instruction to insure that the buffered I/O is available for transfer. Upon interrogation, the buffered I/O responds either affirmative or negative. If the response is affirmative, the central processor immediate branches into a programmed subroutine and interrogates later. After the successful completion of a PCB order, execution of the PDT order can start if desired. The PDT order consists of words which first interrogate a particular read-write channel, then a particular peripheral control unit. Once the central processor finds that it can communicate with the peripheral control unit, it issues a code which selects a particular external device connected to the PCU and the

transaction takes place. When activated by the PDT instruction, the buffered input/output operates completely independent of the central processor. A transaction can only be terminated by three means:

Buffered I/O terminates transaction when word count reaches zero.

External device terminates with End of Order if initial word count is zero.

Power failure interrupt will terminate action.

Seven codes are available for the PCU to specify action to be executed by the read-write channels. These are interpreted by the central processor as:

- No action - RWC to/from PCU Data Transfer Idle.
- End of Order Transfer - Release RWC from PCU.
- Frame Demand for Normal Output Transfer - Output data to PCU.
- Frame Demand for Normal Input Transfer - Increment current address, input data from PCU.
- Row Demand Normal - Starting address to current address location, repeat previous data transfer cycle to PCU.
- Frame Demand for Special Output Transfer - Maintain present current address, repeat transfer of last output data to PCU.
- Frame Demand for Special Input Transfer - Decrement current address, read data backwards from PCU.

The buffered input/output channel consists of these major sections: read-write channels, program control logic, and timing and control. Figure 9 emphasizes these major groups and shows the functional blocks within each group. Each functional block will be described below. Connection letters correspond to letters on the central processor diagram.

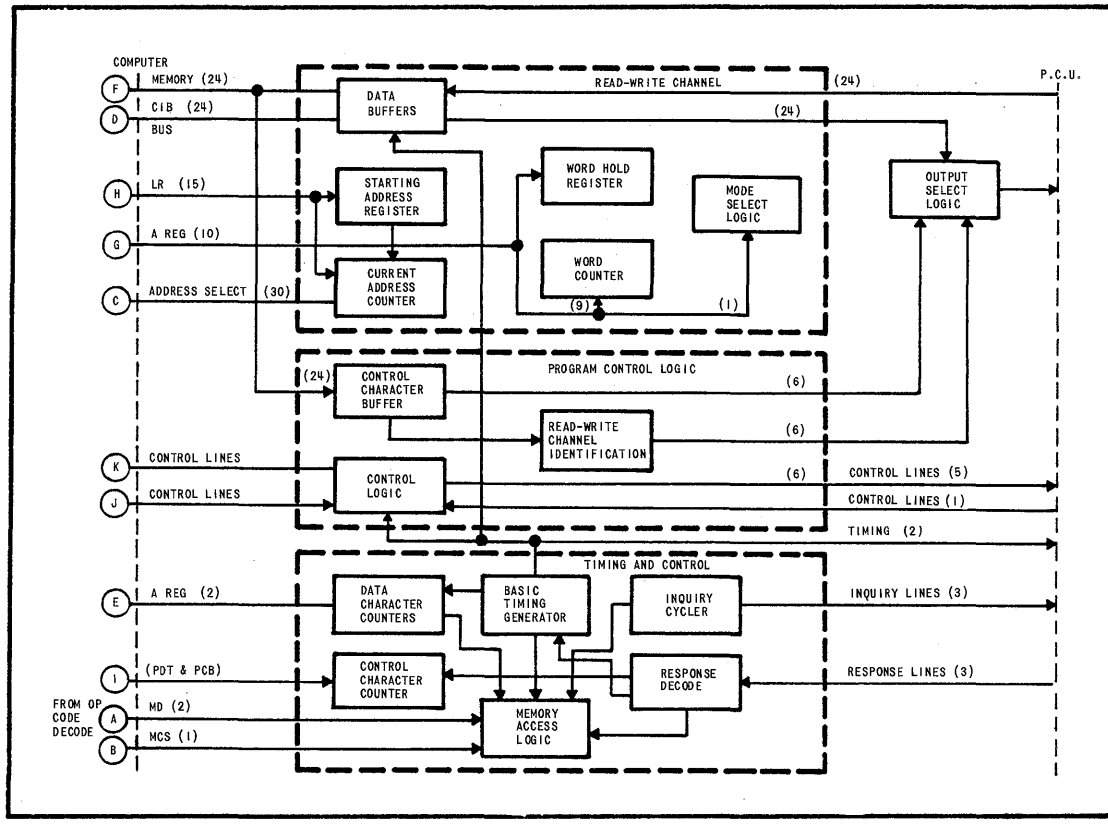


FIGURE 9. THE BUFFERED INPUT/OUTPUT CHANNEL.

READ-WRITE CHANNEL

Data Buffer Registers - store data being transferred between main memory and external devices. There are two registers. One is used to transfer information in 6 or 24 bits from memory to external device. Information being transferred from external device to main memory is first placed in this register, then dropped into the second register before being transferred into memory. This frees the first register for new data. The second register also assembles information into proper format before transferring the data into main memory.

Starting Address Register - is loaded with the memory starting position where transfer is initiated. A Row Demand Normal response causes the register contents to be shifted to the Current Address Counter.

Current Address Counter - is an up-down counter that indicates the read or transfer location in memory. It counts word by word from the initial position of transaction.

Word Counter - records the number of words being transferred.

Word Hold Register - holds the initial word count upon receipt of a Row Demand Normal response and transfers its contents into the word counter.

Mode Select Logic - sets the read-write channel for either a 6 or 24-bit mode of transfer.

PROGRAM CONTROL LOGIC

Control Character Buffer - is a 24-bit shift register that holds the P characters of the PCB or PDT orders (see instruction list). It is loaded directly from the M register. This information is used to check RWC status, select a particular peripheral control unit, and interrogate or issue control information to a particular external device.

Control Logic - allows external devices and central processor to communicate for buffered I/O operation during PCB and PDT executions.

Read-Write Channel Identification - is a 6-bit register that holds the first P character of a PDT instruction. It is loaded from the control character buffer. Upon completion of the PDT order the contents are sent to the addressed peripheral control unit.

TIMING AND CONTROL

Two Data Character Counters - keep track of data being transferred between buffered I/O and external devices, and assembles the data words in the data buffers into the correct format for partial data transfer.

Control Character Counter - contains the actual number of P characters that have been transferred on a particular word of a PCB or PDT order.

Basic Timing Generator - is a six-stage shift generator controlled by the three-megacycle clock in the central processor. It supplies all timing for the buffered input/output channel.

Memory Access Logic - demands memory access for word transfer. Upon demand, the central processor acknowledges and informs the access logic of the memory status.

Inquiry Cycler - is a three-stage shift counter which samples a peripheral control unit every six microseconds for action requests.

Response Decode - decodes the information from the peripheral control units which specify actions to be performed by the read-write channel.

INTERRUPTS

Interrupts are a means of halting the computer at a convenient point during operation for sub-sequence execution. *ALERT* has both internal and external interrupt capability. The basic computer uses three levels of internal interrupts, but has provisions for eight levels. Eight levels are provided for external purposes. External interrupts may be expanded to 24 levels.

INTERNAL INTERRUPTS

Internal interrupts have absolute priority and cannot be blocked. The three types included in the basic *ALERT* are power failure, trapped orders, and control error. These are listed in order of priority. A brief description of each follows.

Power Failures - require a one millisecond warning supplied by the power supply that primary power is failing. During this interval the instruction being executed is completed and a sub-sequence is obtained from a predetermined location in memory. The completion of the order being executed sets the sequence register to the address of the next normal instruction. No information is lost during this process. When primary power is stable again, normal operation is resumed.

Trapped Orders - are decoded op-codes with no built-in hardware. There are provisions for 18 trapped op-codes for programmer use. A trapped order causes a sub-sequence to a predetermined memory location common to all 18 trapped orders. This location usually contains an instruction which stores the program counter and then initiates a jump to a subroutime. By using trapped orders, operations such as square root may be performed with considerably less hardware.

Control Error Interrupts - may be generated by two means: PDT order failure or emergency external interrupt. Emergency external interrupts are activated by external devices that must obtain computer access. An example is loss of information if access is not gained immediately. Each of these interrupts causes a sub-sequence.

EXTERNAL INTERRUPTS

ALERT has eight external interrupts which service external devices. Each interrupt has a sub-sequence in a predetermined memory location, and action will be taken according to sub-sequence. The use of these interrupts depends upon the requirements of the external devices and the program being executed. The interrupt system automatically generates a

sub-sequence address for each of the eight interrupt lines to external devices. A fixed priority for interrupt is established and the computer can selectively mask then block each line. Priority is established by the interrupt mask register corresponds bit-for-bit with the interrupt register. To allow programmed blocking, only the inputs to the interrupt register which correspond to the mask register can cause a sub-sequence; the others will be disabled. The mask register may be loaded from memory by executing the LIM instruction or its contents may be exchanged with memory by the SML instructions.

External interrupts are serviced according to priority. Lower priority interrupts are blocked by the higher priority sequence but held in the interrupt logic until the block is reset by execution of the SRB or RSS instructions. The block may also be set by programming, the SRB or RSS instructions. Once the block is reset, the next interrupt may be serviced.

The interrupt signal is a steady level which enters *ALERT* through the direct input/output channel. Provisions can be made for interrupts to enter by the buffered input/output channel. These signals are not automatically reset but may be reset by program. Status testing orders, such as PCB for buffered I/O testing or SKC for the direct input/output channel will also reset the interrupt signals.

To increase coverage of interrupt lines, more than one external device may be serviced by the same line by external buffering. A scanning subroutine using the SKC, ALR, or PCB instruction may be used to determine interrupt priority when more than one external device is sharing an interrupt line.

MEMORY

The basic *ALERT* contains a nondestructive readout (NDRO), word-oriented memory comprised of 4,096 twenty-four bit words electrically alterable by program control (hot data). Modular expansion may be made to 32,768 words in 2,048 word increments. A hot data memory is included in the basic *ALERT*, but cold data storage is an available option. Cold data is information preloaded by external loading devices.

Storage elements are miniature biax cores in a two-wire configuration. Relatively low power is required to read or write. The following discussion describes the element, its use in the memory scheme, and circuitry required to use it.

BIAX ELEMENT

The biax element is a block of ferrite containing two orthogonal nonintersecting holes (see Figure 10). The smaller hole is threaded with an interrogate winding and the larger with a sense winding. Information is stored by impressing a bipolar signal on the interrogate winding simultaneously with an information signal impressed on the sense winding. This orients the flux to represent either a one or a zero as determined by the polarity of the information signal. To read the stored information, an interrogate pulse is impressed on the interrogate winding and a signal results on the sense winding with polarity representing the stored one or zero (refer to Figure 11).

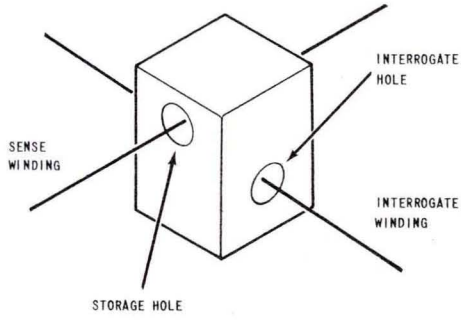


FIGURE 10. THE BIAX ELEMENT SHOWING HOLE LOCATION.

MEMORY PLANE

The biax elements are mounted on both sides of multilayer printed circuit boards as shown in Figure 12. One side of a plane contains 256 words grouped into four 64-word fields. Each word field contains 24 biax elements per word. A common sense winding is passed through corresponding bits of each word. An interrogate winding passes through each element of a word. Both ends of each interrogate winding are connected to a 64 by 64 selection matrix (see Figure 13). These are designated as y, x and $\overline{x}$ busses and are selected by transformer matrixes with the x and y select circuitry. Connections to the x and $\overline{x}$ busses are through diodes, so that bipolar current pulses may be used for writing and unipolar pulses for reading. Word selection lines are internally connected within the multilayer board to minimize external connections.

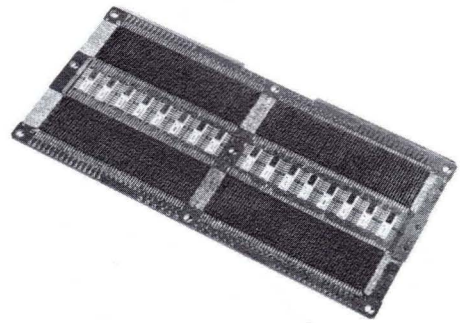


FIGURE 12. A MEMORY PLANE.

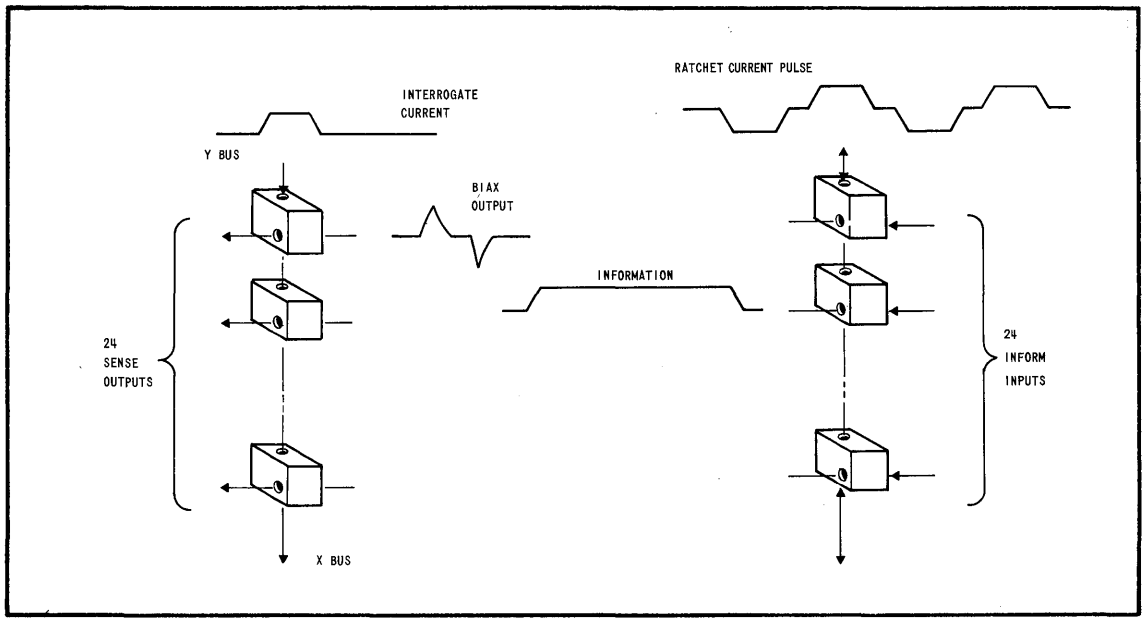


FIGURE 11. READ AND WRITE SIGNALS FOR BIAX ELEMENTS.

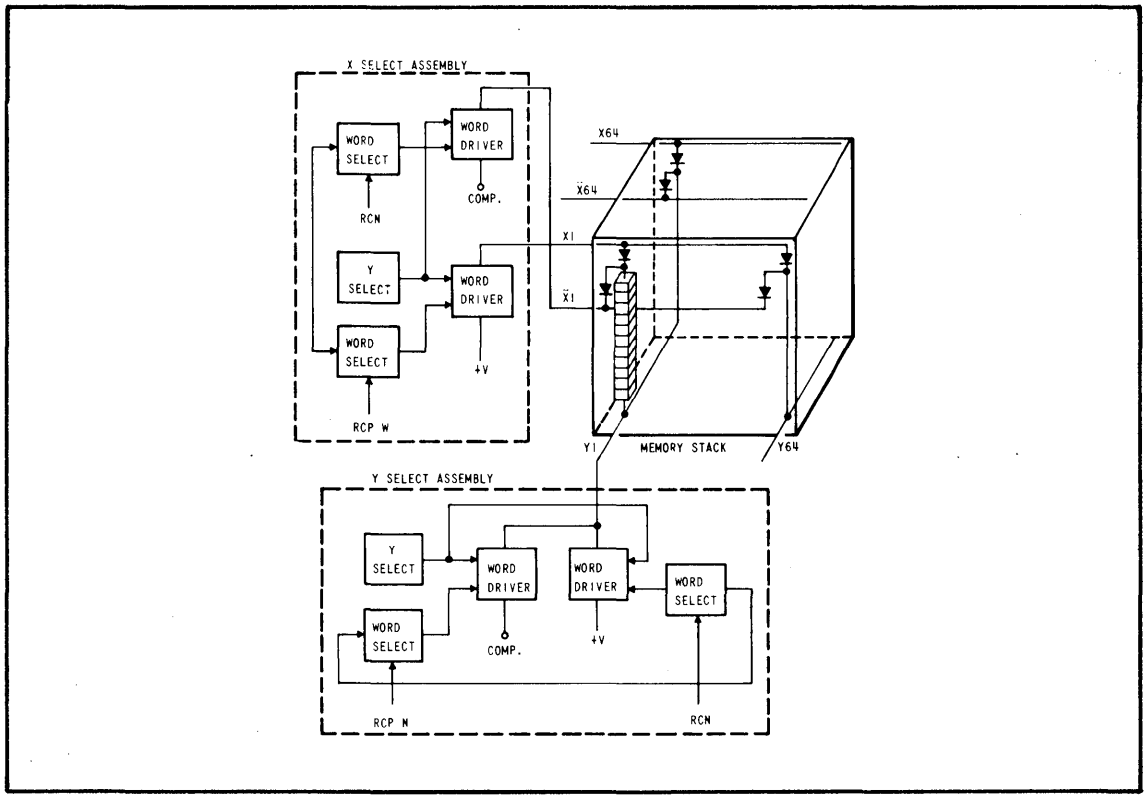


FIGURE 13. THE SELECTION MATRIX SHOWING X AND Y SELECT ASSEMBLIES.

MEMORY STACK

Eight memory planes comprise a 4,096 word memory stack. Sense windings are split into two 24-line groups to reduce inductive loading and permit a faster write cycle. Each sense winding originates at a sense amplifier and is threaded as shown in Figure 14. Note that after the winding has passed through elements on one side of each board it is connected to an information driver then is passed through elements on the opposite side of each board. Forty-eight sense amplifiers and 48 information drivers are employed.

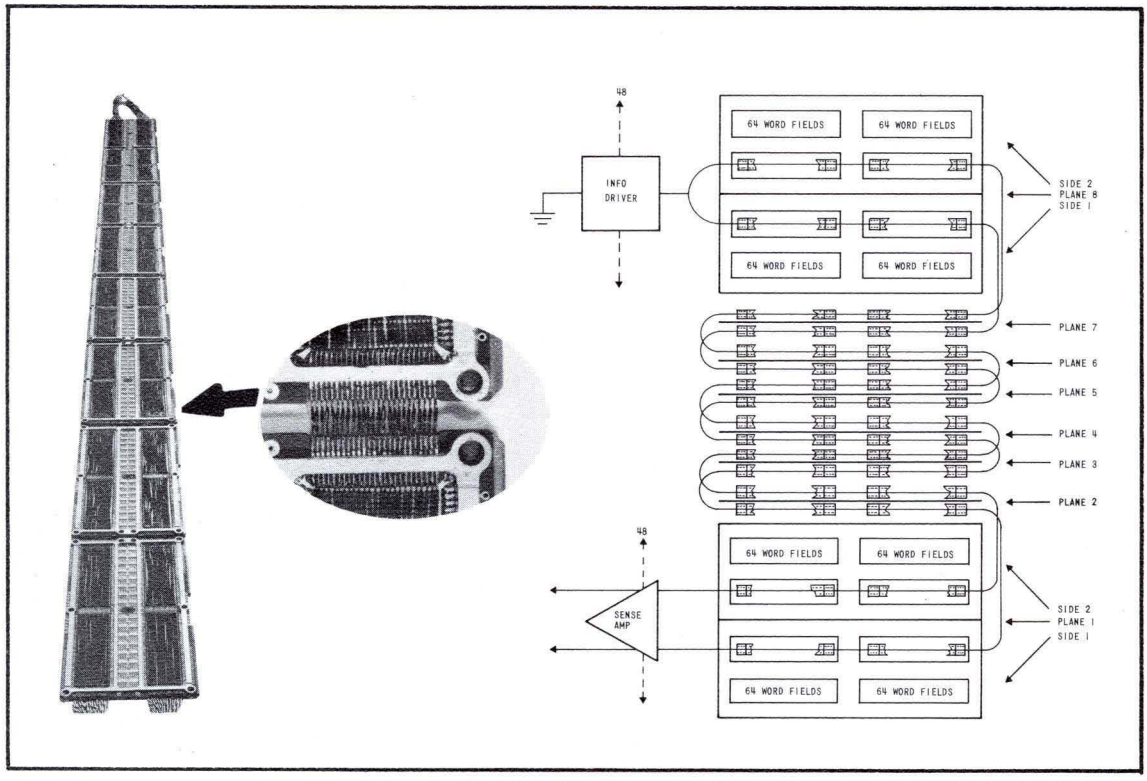


FIGURE 14. THE MEMORY STACK SHOWING SENSE WINDINGS.

MEMORY OPERATION

The memory stack and associated electronics is shown in block form in Figure 15. Memory operation may be grouped by function: select, read and write, timing and control, and compensation. The stack has been discussed previously. Each block will be described briefly by function.

Selection. Word selection is performed by addressing the x and y select assemblies. Groups of words are selected by the assemblies and the particular word desired is located by coincidence of the x and y busses at a unique point within the group.

Read and Write. One sense amplifier is connected to each sense line and amplifies the biax element output when the element is being read. The sense amplifies are high gain, wide bandpass circuits so that the high frequency signals may be faithfully reproduced.

An information driver is also connected to the sense line. It drives bi-directional write current through the line when enabled by a write-enable command and supplied with write information.

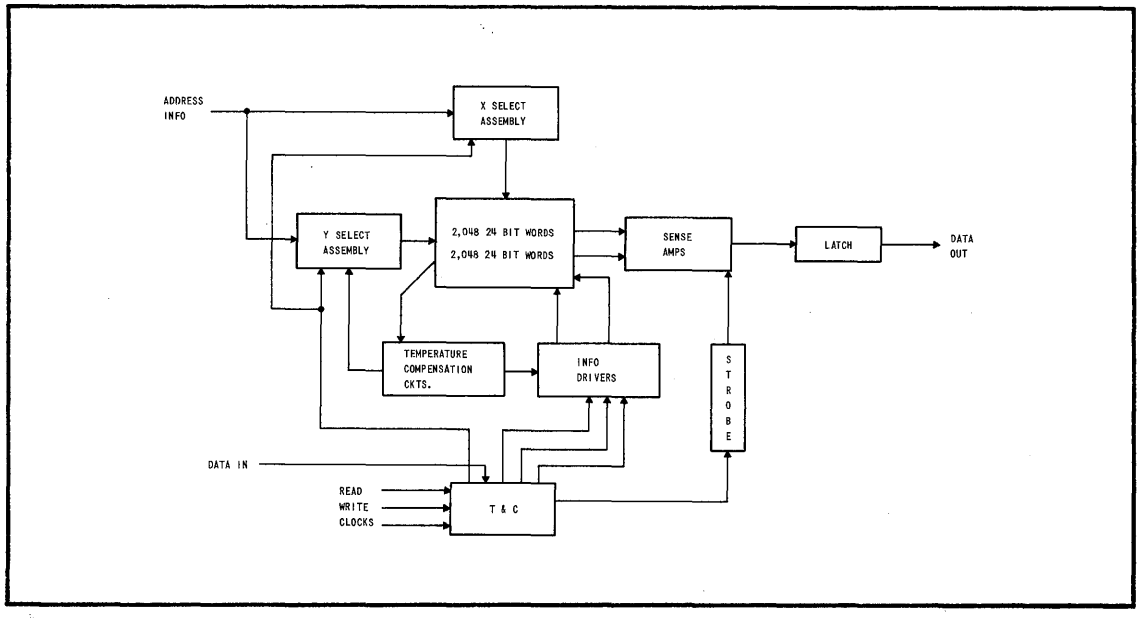


FIGURE 15. THE MEMORY STACK AND ASSOCIATED ELECTRONICS.

Timing and Control. This circuitry operates in conjunction with the three phase, three megacycle clock in the central processor. It receives read or write instructions from the central processor and clocks information in or out of the memory stack as directed.

An integral part of the timing and control circuitry is the strobe generator. It is used to compensate for inherent propagation delays in the sense lines, which have transmission line characteristics. The strobe samples a portion of a signal being read to determine its polarity so that the latches may be set to the proper state.

Compensation. Memory stack temperature is sensed and the compensation circuitry controls the interrogate, ratchet pulse and information current levels over a specified temperature range. This level control prevents disturbance to other biax elements when selected elements are being written into.

WRITING INTO MEMORY

A simplified diagram of the read, write and selection scheme is shown in Figure 16. After a word is located by addressing the x and y selection circuitry and establishing coincidence, the memory is ready to be written into. Word drivers associated with the established point in memory are supplied with ratchet-clock pulses and produce a bipolar current flow in the selected word line. This current flows through each element of the word. A write enable pulse is applied to the information drivers connected to the sense lines which pass through the elements to be written into. The information drivers also receive information pulses with polarity corresponding to ones or zeros. The combined action of the ratchet pulse in the interrogate line and the information pulses in the sense lines causes the biax element flux to orient to the proper position to represent the desired information. Although the information pulses pass through all elements, only the word elements supplied with a ratchet pulse will be written into.

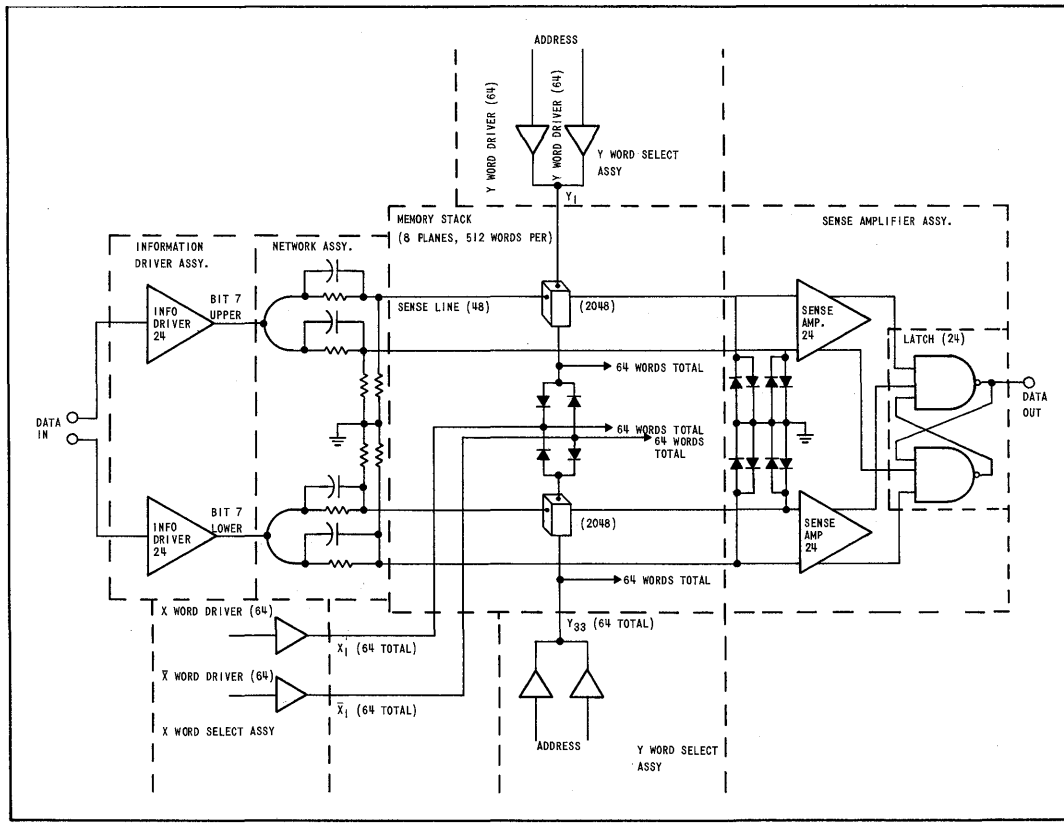


FIGURE 16. READ, WRITE, AND SELECTION SCHEME.

READING FROM MEMORY

Word selection for reading is as described for writing. After selection is made, a unipolar interrogate current is passed through the interrogate line associated with the selected word. Signals are induced into each sense line with polarity representing the stored ones or zeros. The signals induced in the sense lines are amplified by the sense amplifiers and leave the memory via the memory bus.

CIRCUIT DESCRIPTION

Circuits in *ALERT* are separated into two categories: Logic and Memory. Microelectronics are used in the central processor logic and in the memory. These circuits are monolithic or hybird integrated flatpacks offering greater reliability at a reduced cost. In the few cases where flatpacks are not feasible, silicon semiconductors are used. The following discussion will describe flatpack construction, the flatpack types used, and memory circuits by function.

LOGIC CIRCUITS

ALERT features the 40-lead microelectronic flatpack, a Honeywell exclusive. All logic circuitry is high level transistor-transistor logic (HLTTL) and is packaged in either 14 or 40-lead flatpacks. By packaging more circuits per flatpack, cost is reduced, reliability increased and less space is required within the computer. The 40-lead flatpacks contain steering arrays and are used to gate signals into flip-flop inputs. *ALERT* uses 239 arrays to perform operations that would require 1,172 conventional flatpacks. A 25 percent increase in MTBF is also gained by using the steering array since all circuits are combined on a single substrate. Cost savings is best illustrated in tabular form (see Figure 17).

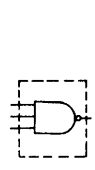
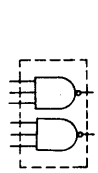
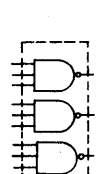
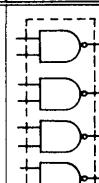
PACKAGE CONTENT	SINGLE GATE	DUAL GATE	TRIPLE GATE	QUAD GATE
				
VALUE TO USER	$5	$10	$15	$20
RELATIVE MANUFACTURING COST	1.0	1.1	1.2	1.2
SELLING PRICE PER NETWORK PACKAGE	$10	$11	$12	$12
EQUIVALENT COST PER CIRCUIT FUNCTION TO USER	$10	$5.50	$4.00	$3.00

FIGURE 17. COST SAVINGS BY USING FLATPACKS.

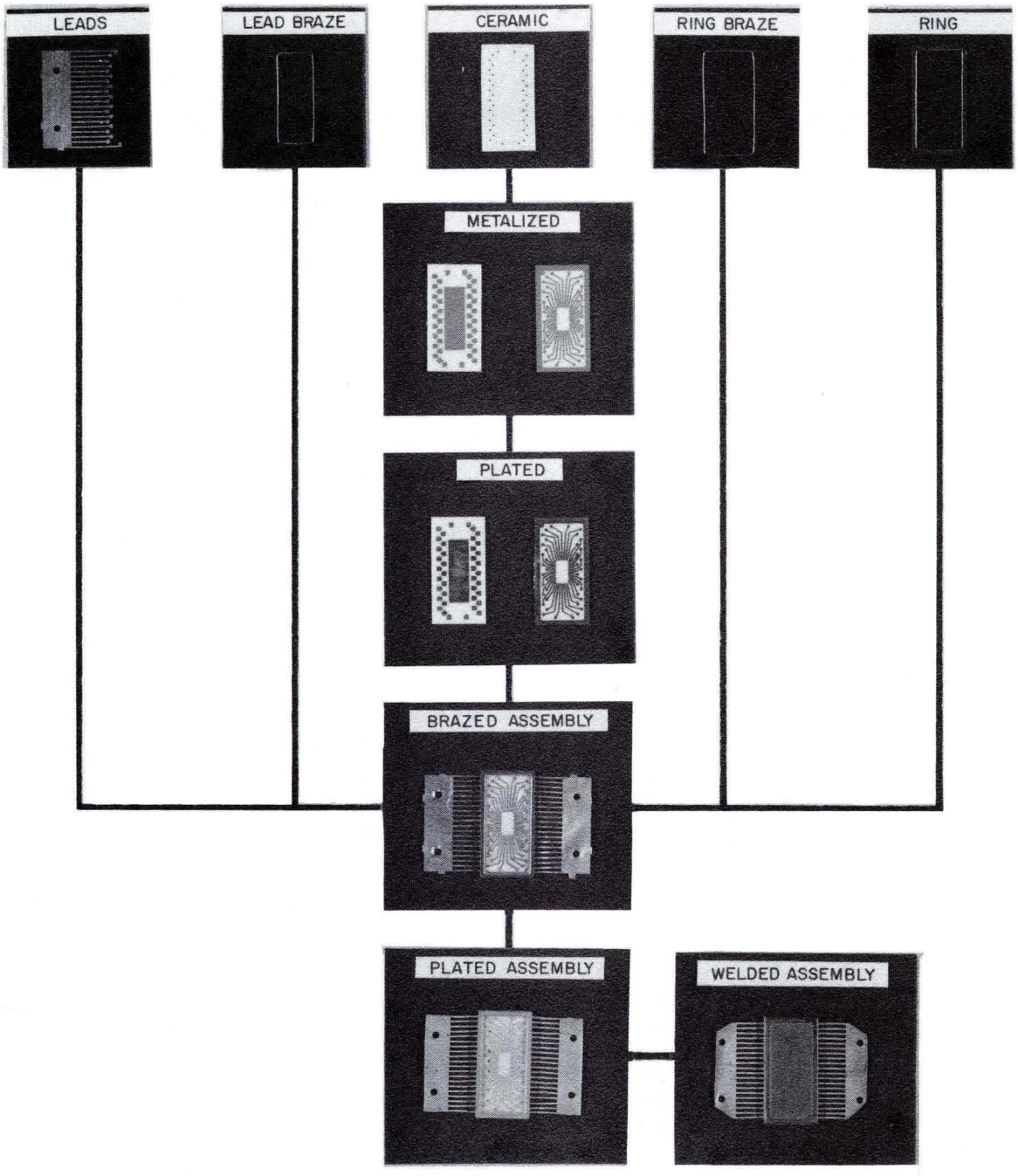


FIGURE 18. STEPS IN FLATPACK CONSTRUCTION.

Circuit Construction. Logic circuit elements are fabricated within monolithic silicon chips by the planar epitaxial process. Individual components within a chip are interconnected by thin-film gold conductors. Each package is gold-plated Kovar metal. Gold leads are ball-bonded or stitch-bonded from metalized pads on the chip to ribbon leads within the flatpack, forming an all-gold monometallic interconnection system. Leads are brought out through the flatpack through glass-to-metal seals and the package is hermetically sealed. The steps to produce a 40-lead flatpack are shown in Figure 18. A group of chips before extraction are shown in Figure 19 with size comparison This chip is extracted and mounted within the package. Both 14-lead and 40-lead flatpacks, with covers removed, are shown in Figure 20.

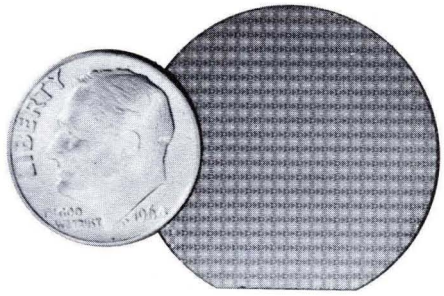


FIGURE 19. MORE THAN 300 CHIPS BEFORE EXTRACTION.

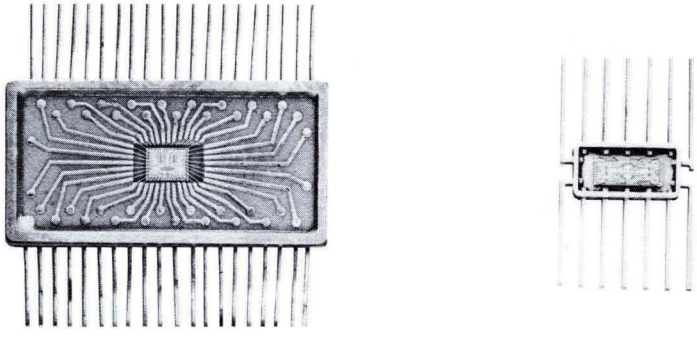


FIGURE 20. A 40 LEAD FLATPACK (LEFT); 14 LEAD FLATPACK (RIGHT).

The improved flatpack design is compared to an earlier design in Figure 21. By using a greater cross-sectional length of glass-to-metal seal, leakage is reduced increasing reliability. In addition, the lead is less susceptible to vibration failures because a more direct path is used and a smooth curve in the wire replaces the sharp bend.

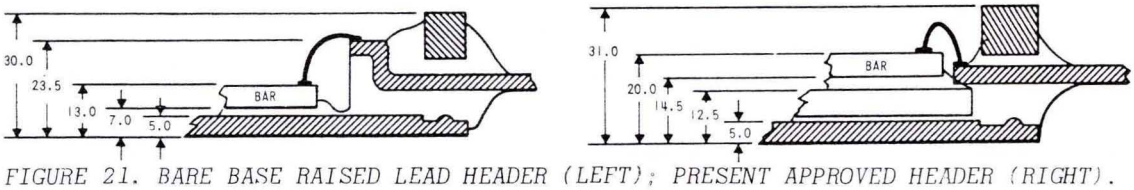


FIGURE 21. BARE BASE RAISED LEAD HEADER (LEFT); PRESENT APPROVED HEADER (RIGHT).

Advantages of *ALERT* Circuits. The HLTTL circuits chosen for *ALERT* offer greater advantages than can be derived from any presently available integrated digital circuits. Some of the outstanding benefits are:

- Double epitaxial construction results in low saturation resistance providing a fan-out capability of 15 with a low saturation voltage. Other logic configurations offer fan-out of only five. This increased fan-out eliminates the need for driver stages reducing overall parts count.

- The basic inverting gate used in the entire family of HLTTL devices is capable of a worst-case noise immunity of 500 millivolts at full fan-out over a temperature range of -55°C to +125°C.

- Low output impedance in both one and zero states results in good dynamic noise rejection.

- Propagation delay through logic gate element may be optimized for a particular application by a choice between propagation time and fan-out size. An average propagation delay of 25 nanoseconds may be obtained by limiting the fan-out to six. The delay average delay at full fan-out is rated at 40 nanoseconds.

- Purple plague is eliminated by the all-gold monometallic interconnection system.

- Extremely small device-- geometry provides a low propagation delay-- power dissipation product.

Logic Circuit Family. *ALERT* uses eight types of logic circuitry. The circuits are listed below and tabulated on the following page. The tabulation includes circuit diagram, logic diagram and brief description of each device. The family includes:

- Dual 4-input positive NAND gate.

- Single 8-input positive NAND gate.

- Quad 2-input positive NAND gate.

- Dual exclusive OR gate with expander input for increasing fan-out.

- Dual 4-input expander gate.

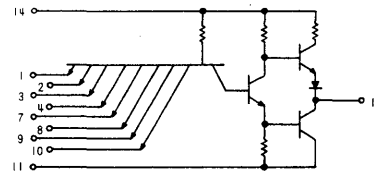
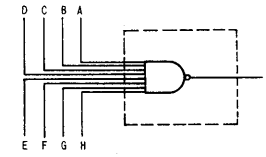
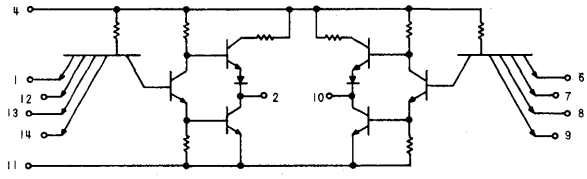
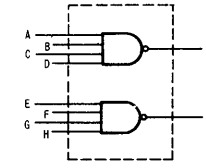
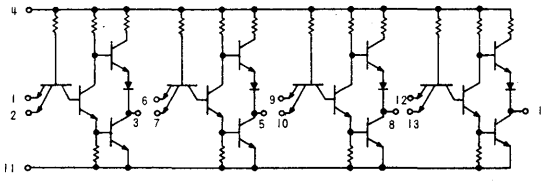
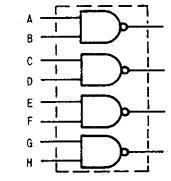
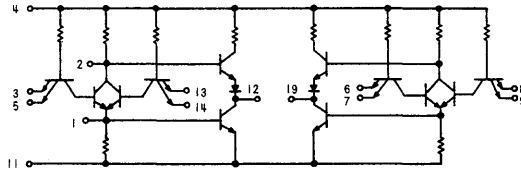
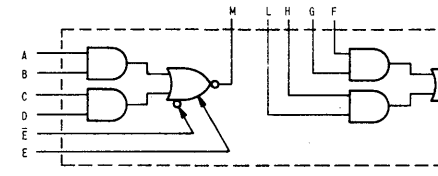
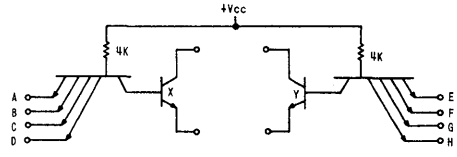
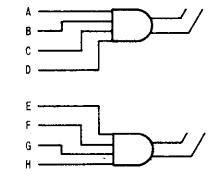
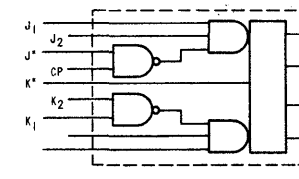
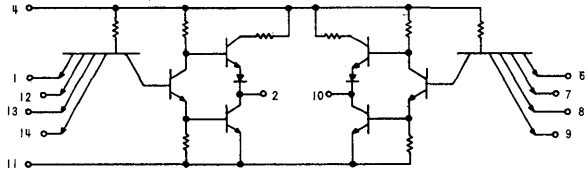
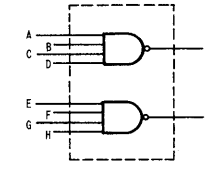
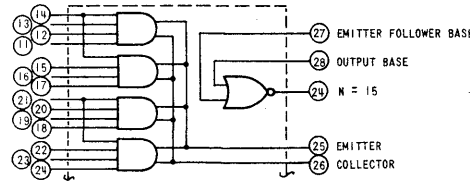
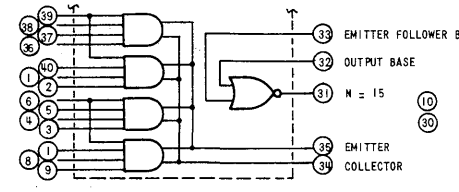
- J-K flip-flop
- Dual positive NAND clock driver
- Steering array.

Memory Circuits

Using the same major functions described previously, the memory is comprised of stack, x and y word select assemblies, information drivers, sense amplifiers, timing and control, and compensation circuitry. The following table lists the number of integrated circuits or silicon semiconductors used:

Circuit	Circuit Type	Number Used
16-Diode Array	Monolithic	512
8-Diode Array	Monolithic	32
Word Driver	Hybrid	128
8-Input NAND Gate	Monolithic	48
Word Select	Monolithic	16
Y Select	Monolithic	8
Information Driver	Thin-film hybrid	48
Rise Time Compensator	Thin-film hybrid	24
Information Driver Diode	Hybrid (6-diode chips)	24
Sense Amplifier Flatpack	Monolithic	48
Sense Amplifier Diode Flatpack	Hybrid (8-diode chips)	24
Tunnel Diode	Discrete component	96
Flip-flop	Monolithic	3
Dual 4-Input NAND Gate	Monolithic	18
Quad 2-Input NAND Gate	Monolithic	10
Single Shot	Thin-film hybrid	8
Memory Clock Driver	Thin-film hybrid	3
Waveform Generator	Thin-film hybrid	1
Waveform Driver	Thin-film hybrid	1
Dual Exclusive OR Gate	Monolithic	12
Differential Amplifier	Monolithic	2
Dual Clock Driver	Monolithic	5

ALERT LOGIC FLATPACKS

CIRCUIT	LOGIC
	
	
	
	
	
	
	
	

	NO. USED	COMMENTS
	172	SINGLE 8 - INPUT POSITIVE NAND GATE - HAS SHORT PROPAGATION DELAY AND HIGH NOISE IMMUNITY. DESIGNED TO OPERATE OVER THE FULL MILITARY TEMPERATURE RANGE OF -55°C TO +125°C
	76	DUAL 4 - INPUT POSITIVE NAND GATE - HAS SHORT PROPAGATION DELAY AND HIGH NOISE IMMUNITY. DESIGNED TO OPERATE FROM -55°C TO +125°C.
	184	QUAD 2 - INPUT POSITIVE NAND GATE - HAS SHORT PROPAGATION DELAY AND HIGH NOISE IMMUNITY. DESIGNED TO OPERATE FROM -55°C TO +125°C.
	66	DUAL EXCLUSIVE OR GATE WITH EXPANDER INPUT - HAS SHORT PROPAGATION DELAY AND HIGH NOISE IMMUNITY. DESIGNED TO OPERATE FROM -55°C TO +125°C. ADDITIONAL INPUTS ARE PROVIDED TO ONE CIRCUIT FOR INPUT EXPANSION.
	23	DUAL FOUR - INPUT EXPANDER GATE - IS DESIGNED TO OPERATE FROM -55°C TO +125°C.
	355	JK FLIP-FLOP - HAS SHORT PROPAGATION AND SETUP TIMES, HIGH NOISE IMMUNITY AND IS DESIGNED TO OPERATE FROM -55°C TO +125°C. NO CIRCUIT DIAGRAM SHOWN DUE TO COMPLEXITY.
	78	DUAL POSITIVE NAND CLOCK DRIVER - HAS HIGH FAN-OUT CAPABILITY AND IS DESIGNED TO OPERATE FROM -55°C TO +125°C.
	239	STEERING ARRAY - LOGIC DIAGRAM IS SHOWN MINUS CIRCUIT DIAGRAM BECAUSE OF COMPLEXITY. IT HAS SHORT PROPAGATION DELAY AND HIGH NOISE IMMUNITY AND IS DESIGNED TO OPERATE FROM -55°C TO +125°C.

PHYSICAL ASPECTS

State of the art packaging techniques have been used throughout *ALERT* mechanical design. The computer is compact, rigidly constructed, and lightweight so that many applications may benefit from this fast, reliable airborne scientific machine. A foremost consideration of the packaging scheme is maintainability. Ease of maintenance will be obvious upon reading the packaging details. Welded component-to-circuit board construction, minimized interconnections by multilayer printed circuit use, and proper thermal design are combined with advanced circuit packaging to increase reliability. All mechanical aspects of *ALERT* will be covered in the following discussion.

PACKAGING

FIGURE 22. MODULAR UNITS SHOWING CENTRAL PROCESSOR (LEFT); MEMORY (RIGHT).

ALERT is housed in a compact, rugged configuration suitable for a variety of applications. The computer is contained in modular units designed to air transport radio (ATR) specifications. For expansion and to add packaging versatility, each major portion of the computer is in a separate housing (shown in Figure 22). The central processor is housed in one unit and different word capacity memories are housed separately so that a memory to meet application requirements may be selected and mated to the central processor. Other members of the *ALERT* family include the buffered input/output unit, power supply unit, and adaptor or interface units for special applications. Each is housed in a separate modular unit and packaging techniques are similar to those to be described for central processor and memory.

FIGURE 23. REAR VIEW OF COMPUTER.

All external connections are made through rack and panel connections on the rear of the units (see Figure 23). For ease of installation and adaptability to various systems, vibration isolation is not required except for the most stringent applications. Cooling may be either cold plate or forced air. Modular unit construction details will show that *ALERT* is designed to be reliable and easy to maintain.

CENTRAL PROCESSOR UNIT

The central processor structure is shown in Figure 24. It consists of an aluminum main frame including base plate, vertical members, and rear connector housing. External connectors are located on the rear; memory unit connectors are on the side. Although memory and central processor are in separate modular units, transactions between the two never have to leave the computer through external connectors.

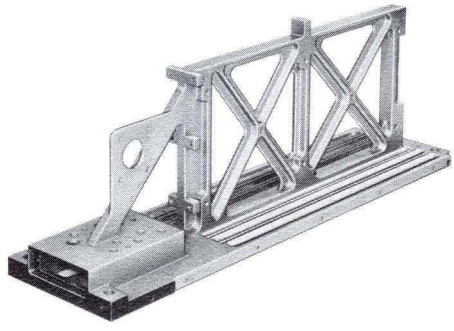


FIGURE 24. CENTRAL PROCESSOR STRUCTURE.

Circuitry within the central processor includes addressing, arithmetic and master timing and control logic. The logic flatpacks are mounted on six, double-sided, multilayer printed circuit boards. A typical board contains 30 layers of circuit paths, comprised of 20 logic layers and 10 layers for voltage, weld, and ground. A board prior to assembly is shown in Figure 25. Figure 26 shows flatpacks being welded.

The complete circuit boards are connected to a multilayer master interconnection board by hinges and flexible jumpers. This hinging arrangement makes each board accessible for test or repair (see Figure 27). The master interconnection board is hinged also to allow the assembly to be secured in the processor housing so that each circuit board is interleaved between metallic, thermally conducting structural members. Figure 27 also shows the assembly pivoted away from the thermal planes and opened for circuit access.

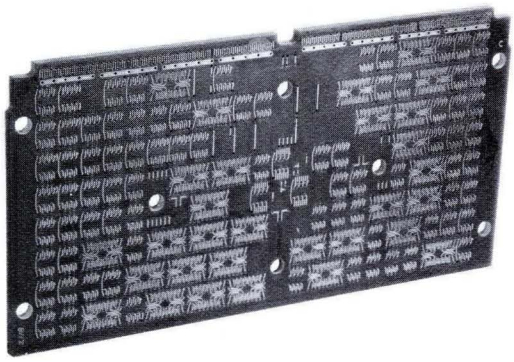


FIGURE 25. LOGIC CIRCUIT BOARD BEFORE ASSEMBLY.

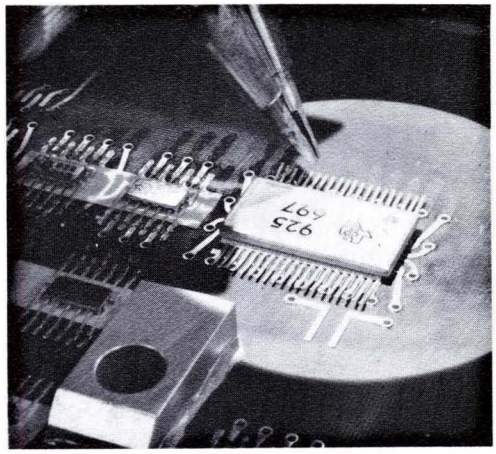


FIGURE 26. FLATPACKS BEING WELDED TO BOARD.

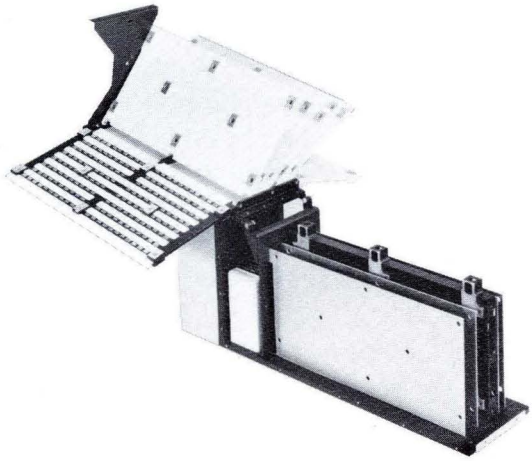


FIGURE 27. CIRCUIT BOARD MOUNTING ARRANGEMENT WITH BOARDS REMOVED.

The assembled central processor unit weighs 19 pounds and occupies 0.43 cubic feet. It is 7.6 inches high, 19.5 inches long and 5 inches wide.

MEMORY UNIT

Packaging is similar for all memory sizes. An aluminum structure for the 4, 096 word memory is shown in Figure 28. This is typical for all word capacities except for size. All connections are made to the central processor as discussed previously.

Within the memory are the following modular subassemblies:

- X word select assembly.
- Y word select assembly.
- Timing and Control.
- 4, 096 word biax stack.
- Information driver assembly.
- Sense amplifiers.
- Compensator assembly.
- Latches.
- Resistor network.

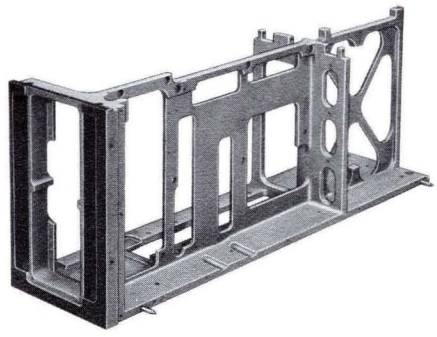


FIGURE 28. STRUCTURE FOR 4,096 WORD MEMORY.

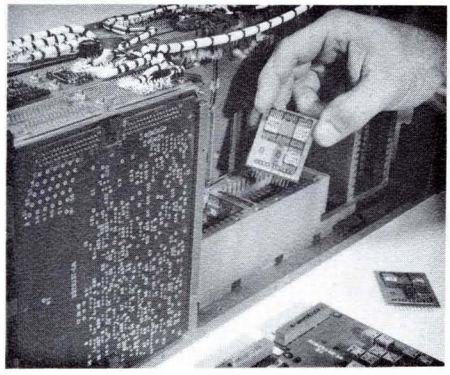


FIGURE 29. SUBASSEMBLIES OPEN FOR EASY ACCESS.

Each of the subassemblies is mounted in the structural frame so that replacement or repair is relatively easy. Figure 29 shows circuit board being installed in the information driver assembly.

The X select, Y select, and timing and control assemblies are similar in construction. Each consists of two multilayer circuit boards mounted on an aluminum frame. The frames are hinged to the main structure and swing upwards for circuit element and test point exposure.

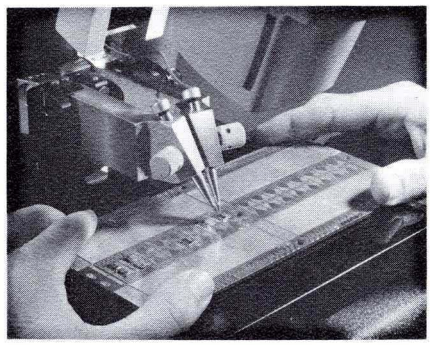


FIGURE 30. FLATPACK BEING WELDED TO MEMORY PLANE.

A 4,096 word memory stack consists of eight memory planes. Each plane is a double-side multilayer printed circuit board with memory elements and diode flatpacks mounted on it. The elements are held in place by potting material. The flatpacks are welded also. See Figure 30. The eight plane boards are bolted together to form the stack. X and Y buses pass through each board and cables connect to the buses. The stack is placed in a metal housing and closed with panels. The housing is rigidly mounted in the memory structure. See Figure 31 for a pictorial view of memory stack.

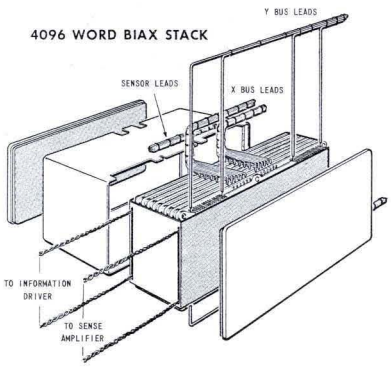


FIGURE 31. MEMORY STACK.

The stack is part of a subset that comprises a replaceable unit. It is hardwired to the information driver, sense amplifier, latch, and resistor network assembly before installation in the memory structure. Both the information driver and sense amplifier assemblies contain 24 smaller amplifier or driver assemblies mounted on a multilayer board. Latch (memory register) and resistor network assemblies are also printed circuit boards. All circuit elements and test points within the replaceable subset are accessible.

Compensation circuitry is mounted on circuit boards housed within the compensator assembly metal frame. All assemblies are interconnected by a cable harness. Expansion was a major consideration of memory unit design. By using a larger frame structure, presently designed modular subassemblies may be added to increase word capacity. The expansion scheme is illustrated in Figure 32.

A 4,096 word memory occupies 0.43 cubic feet and weighs 18 pounds. Its dimensions are 7.6 inches by 19.5 inches by 5 inches.

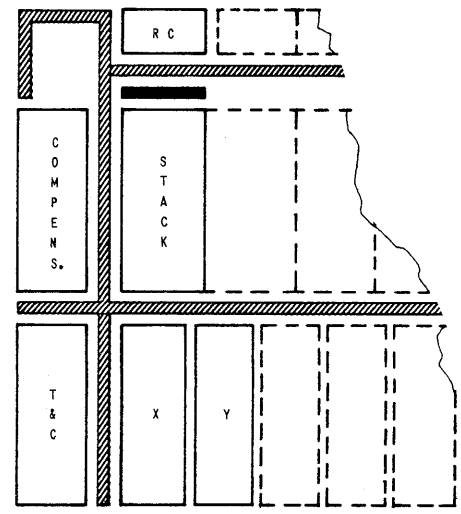


FIGURE 32. EXPANSION SCHEME FOR MEMORY UNIT.

ENVIRONMENTAL CHARACTERISTICS

ALERT is designed to operate in the severe environments imposed by aircraft or missile applications. Military specifications governing its design are MIL-E-5400 and MIL-I-26600. The latter specification outlines shielding requirements for radio frequency interference.

Cold plate or forced air cooling allows *ALERT* to operate over a temperature range of -55°C to +85°C. Storage temperature may range from -62°C to +100°C. Other characteristics include:

- Linear Acceleration (nonoperating)

  15g in any axis

- Sinusoidal Vibration (operating)

5 - 10 cps	0.08 inch Double Amplitude
10 - 15 cps	±0.42g
15 - 71 cps	0.036 inch Double Amplitude
71 - 500 cps	±10g

- Random Vibration (operating)

20 - 200 cps	$0.12g^2$/cps
200 - 500 cps	$0.20g^2$/cps
500 - 800 cps	$0.09g^2$/cps
800 - 2,000 cps	$0.05g^2$/cps

- Shock (nonoperating)

  50g peak acceleration

  3 shocks along three orthogonal axes

RELIABILITY

Reliability has been one of the most important design parameters for *ALERT*. A mean-time-between-failures (MTBF) goal has been set at 10,000 hours. Honeywell is well on its way to attain this goal. A comprehensive reliability plan encompassing every aspect of the design and production, resulted in an exceptionally high MTBF. Some of the steps that have aided this achievement are:

- Extensive use of integrated circuits.
- Development of multifunction integrated circuit chips.
- Extensive use of multilayer printed circuit boards.
- Use of welded connections wherever pssible.
- Specification of only high reliability components.
- Comprehensive circuit stress analysis.

To best illustrate *ALERT* reliability, Tables 1 and 2 show current predictions for both processor and memory. Failure rates were derived from MIL-HDBK-217, FARADA, Honeywell and vendor data. For semiconductors, glass capacitors and film resistors temperature/failure rate relationships were derived by using the Arrhenius mathematical model* as applied to accelerated stress testing.

* See Proceedings of Second Annual Symposium on the Physics of Failure in Electronics, 25 September 1963.

TABLE 1. ALERT MEMORY RELIABILITY PREDICTION.

Item	Estimated Average Stress %	Quantity	Temperature					
			25°C	55°C	70°C	25°C	55°C	70°C
			Percent/1,000 Hours Failure Rate			Total Failure Rate		
Integrated Circuits Mono (14 lead)		213	0.0009	0.0021	0.003	0.192	0.447	0.639
Integrated Circuits (Hybrid)								
2 chip		512	0.0018	0.0042	0.006	0.922	2.150	3.072
3 chip		131	0.003	0.0065	0.009	0.393	0.852	1.179
5 chip		1	0.0045	0.011	0.015	0.005	0.011	0.015
6 chip		51	0.006	0.013	0.018	0.306	0.663	0.918
8 chip		9	0.008	0.017	0.024	0.072	0.153	0.216
10 chip		50	0.01	0.022	0.030	0.500	1.100	1.500
17 chip		25	0.017	0.037	0.051	0.425	0.925	1.275
Solder Joint		4,000	0.000052	0.00011	0.00016	0.208	0.440	0.640
Weld		25,000	--	0.000015	--	0.375	0.375	0.375
Sensor - Thermistor		1	0.010	0.022	0.030	0.010	0.022	0.030
Transistor (power)	20	48	0.008	0.019	0.026	0.384	0.912	1.248
Diode (power)	20	44	0.004	0.009	0.013	0.176	0.396	0.572
Capacitor (solid tant.)	30	49	0.008	0.013	0.018	0.392	0.637	0.882
(wet tant.)	30	12	0.001	0.002	0.003	0.012	0.024	0.036
(glass)		24	0.00065	0.0014	0.002	0.016	0.034	0.048
(ceramic)		171	--	0.001	--	0.171	0.171	0.171
(paper)		5	--	0.001	--	0.005	0.005	0.005
Resistor (GP Film and comp)	<10	82	0.0035	0.0007	0.001	0.029	0.057	0.082
(precision film)	<10	36	0.0082	0.019	0.026	0.295	0.684	0.936
(wire wound)	20	8	0.016	0.020	0.023	0.128	0.160	0.184
(prec. wire wound)	<10	3	0.093	0.105	0.114	0.279	0.315	0.342
Transformers (power)		4	0.050	0.050	0.050	0.200	0.200	0.200
(hi-rel)		256	--	0.003	--	0.768	0.768	0.768
Choke (power)		7	--	0.050	--	0.350	0.350	0.350
Connector - Pins		495	--	0.0013	--	0.644	0.644	0.644
Memory - Elements		102,400	--	10^{-6}	--	0.102	0.102	0.102
					Totals	7.359	12.597	16.429
					MTBF	13,589	7,938	6,087

Note: -- indicates same failure rate as listed under 55°C.

TABLE 2. ALERT CENTRAL PROCESSOR RELIABILITY PREDICTION.

Item	Estimated Average Stress %	Quantity	Temperature 25°C	55°C	70°C	25°C	55°C	70°C
			Percent/1, 000 Hours Failure Rate			Total Failure Rate		
Integrated Circuits Mono (14 lead)		960	0. 0009	0. 0021	0. 003	0. 864	2. 016	2. 880
Integrated Circuits Mono (40 lead)		238	0. 0014	0. 0031	0. 0045	0. 333	0. 738	1. 071
Integrated Circuits (Hybrid) 5 chip		20	0. 0045	0. 011	0. 015	0. 090	0. 220	0. 300
1 chip		2	0. 0009	0. 021	0. 003	0. 002	0. 042	0. 006
Solder Joint		5, 000	0. 000052	0. 00011	0. 00016	0. 260	0. 550	0. 800
Weld		28, 000	--	0. 000015	--	0. 420	0. 420	0. 420
Thermistor		13	0. 010	0. 022	0. 030	0. 130	0. 286	0. 390
Capacitor (solid tant.)	<10	51	0. 004	0. 006	0. 008	0. 204	0. 306	0. 408
(solid tant.)	30	6	0. 008	0. 013	0. 018	0. 048	0. 078	0. 108
(ceramic)	<10	42	--	0. 001	--	0. 042	0. 042	0. 042
Resistor (GP Film)	<10	130	0. 00035	0. 0007	0. 001	0. 045	0. 091	0. 130
(GP Film)	40	4	0. 001	0. 002	0. 004	0. 004	0. 008	0. 016
Connector - Pins		105	--	0. 0013	--	0. 137	0. 137	0. 137
RFI Filter	<10	18	0. 001	0. 001	0. 001	0. 018	0. 018	0. 018
Frequency Standard		1	0. 078	0. 100	0. 127	0. 078	0. 100	0. 127
					Totals	2. 675	5. 052	6. 853
					MTBF	37, 383	19, 794	14, 592

Note: -- indicates same failure rate as listed under 55°C.

Further increases in reliability are expected by:

- Substituting integrated circuits for the remaining discrete parts as technology advances.
- Substituting monolithic for hybrid integrated circuits as the former become available.
- Developing more reliable hybrid circuits by decreasing the number of individual chips per circuit, thereby reducing internal bonds, etc.
- Eliminating internal bonds in integrated circuits by developing a one-step metalization/interconnect system.
- Substituting welds for remainder of soldered connections.
- Maintaining an effective closed loop failure recurrence prevention program to insure rapid corrective action for all problems encountered during production, test and field operations.

MAINTAINABILITY

Computer design eliminates or greatly reduces the need for special skills, training, tools, or test equipment. Specific maintenance features include:

- Unitized packaging and modular plug-in construction.
- Self-test with Go-No Go indication.
- Extensive use of integrated circuitry.
- No scheduled replacement of devices.
- No adjustments or calibrations required.
- All parts are accessible and identified.

As is shown in the packaging discussion, the computer is modularly packaged in line replaceable units (LRUs). Maintenance may be performed at three levels: flight line (organizational), intermediate, and depot. These levels are illustrated in Figure 33.

Flight line maintenance is conducted with self-test and diagnostic routines and circuits within the airborne equipment. No support equipment or special tests sets are required and maintenance can be performed under any operational or environmental conditions. Line replaceable units may be interchanged without requiring manual adjustments, compensation, memory loading, or calibration. For aircraft applications, a Go-No Go indicator located in the cockpit will indicate discrepancies at a confidence level of at least 90 percent.

Intermediate maintenance will depend upon available facilities, equipment and personnel skills. Support equipment and diagnostic routines may be used to isolate malfunctions to the plug-in board within the LRU automatically. After the malfunctioning assembly has been replaced, its operation will be verified by the support equipment. A central processor and memory unit may be used in conjunction with a computer test unit to provide diagnostic capability which would otherwise have to be duplicated in the support equipment.

Isolation, removal and replacement of integrated circuits may be performed at either intermediate or depot level. Honeywell suggests the repair be made during intermediate maintenance to reduce storage of spare boards.

Malfunctioning LRUs not repairable at the two previous levels will be returned to depot or factory. Memory stacks requiring major repair must be returned to depot because of high density packaging. Since the other units in the computer can be repaired at the intermediate level, reduced depot maintenance can be assured.

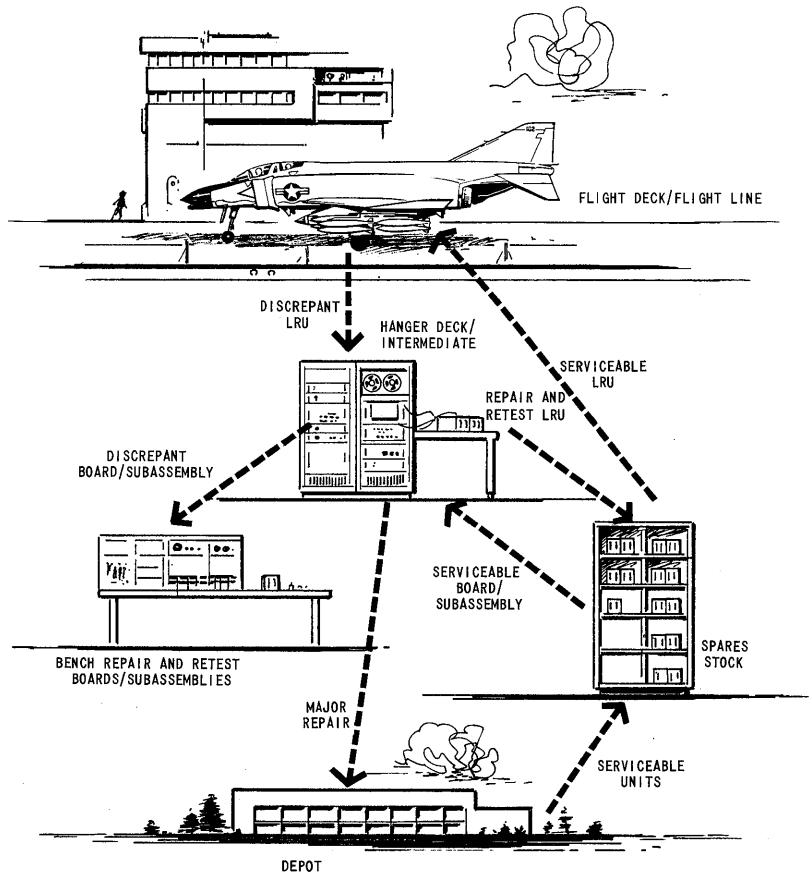


FIGURE 33. MAINTAINABILITY SCHEME.

PROGRAMMING THE ALERT

Sufficient software and efficient instructions make *ALERT* a fast, versatile computer. Two standard but separate software systems are supplied at no additional cost with each computer. One system includes a group of basic programs to be executed on *ALERT*. This group consists of an assembly program, operational subroutines (both real-time and nonreal-time), utility and confidence test programs. The other system is a support group written for the Honeywell 800 scientific computer for use in development of *ALERT* operational programs. This system includes assembler and simulator programs.

To illustrate *ALERT* execution ability, it is compared with 13 competitive machines in Table 3. Basis of comparison is a sample problem generated and evaluated by an independent source. The sample problem programming is documented by Honeywell and is available upon request (Honeywell Aero Document R-ED 28168, 4 January 1964).

TABLE 3. RESULTS OF SAMPLE PROBLEM PROGRAMMING.

Element of Program	Machine Nos. 1	2	3	4	5	6	7	8	9	10	11	12	13	*ALERT*
Time														
Δ_1 *	213,000	64,790	184,807	36,424	81,424	22,969	31,584	69,179	19,943	377,600	63,000	591,360	881,020	18,030*
Major Loop I - Step 1	73,700	8,205	63,668	1,370	**	**	3,933	**	4,266	61,530	2,988	50,449	85,680	1,980
Steps 2 - 21	18,900	4,595	15,250	3,464	6,507	2,109	2,531	6,251	1,670	37,740	6,048	42,574	61,180	1,443*
Major Loop II	15,100	5,040	12,611	2,776	6,720	1,260	1,290	3,162	1,898	30,161	3,372	31,336	50,820	1,611
Major Loop III	14,100	4,470	17,972	2,725	9,951	1,573	3,835	6,128	2,174	35,920	3,240	86,132	140,840	2,045
Minor Loop	4,000	1,588	3,583	718	1,366	466	598	1,412	334	5,200	1,404	10,418	15,120	246*
Interrogation	11,700	1,302	4,250	112	1,769	547	966	1,326	337	7,680	408	8,121	13,720	484

NOTE: The numbers in the matrix represent microseconds.

* Δ_1 is defined to be the time between successive entries to Jamor Loop, Step 2. It is roughly equivalent to five passes through Major Loop I, Steps 2 through 21, one pass through Major Loop II, two passes through Major Loop III, one pass through the Interrogation Loop, and fifteen passes through the Minor Loop.

** This step was not done.

ALERT SOFTWARE SYSTEM

ALERT may be efficiently applied to many applications by using this system consisting of assembler, operational subroutines, utility and confidence test programs. The assembler is a programming tool for translation of symbolic language into machine language (binary). Programmers may use mnemonic names for operation codes and assign names to specific data groups or items for operand reference. An additional benefit of the assembler is pseudo-operations for expressing concepts having no

counter-part in normal machine language. Operational subroutines provide a library of basic mathematical routines available for repeated use. The subroutines are divided into real-time and nonreal-time packages for the programmer's convenience. Utility programs provide flexibility in loading and debugging object programs and confidence test assures operation without malfunction by denoting faulty computer units. Each system component will be discussed more fully.

SYMBOLIC NOTATION ASSEMBLY PROGRAM (SNAP)

SNAP provides a running program complete with memory allocation from English-Algebraic shorthand coded information. Provision is made for detection and correction of errors. The system will assemble symbolically coded programs from paper tape input into bi-octal paper tape output information. This information may then be loaded into magnetic core storage by either the *ALERT* bootstrap or a relocatable loader included in the computer service package. The printer produces a listing of symbolic card numbers for editing, output machine mode with relocatable or absolute locations, and input symbolic coding with remarks.

Programs prepared in SNAP closely resemble machine-coded programs but offer the additional benefit of being readable without reference to charts or tables.

OPERATIONAL SUBROUTINES

These subroutines are contained in two off-the-shelf packages. A real-time package includes subroutines optimized by special programming techniques for expedient execution. Nonreal-time subroutines group more conventional calculation methods, such as Taylor series and polynomial approximations. In general, these subroutines require less computer storage but more computer calculation time. Typical execution time/storage trade-offs between the two packages are illustrated below:

Subroutine	Package	Storage (words)	Execution Time (μsec)
SIN/COS	Real-Time	209	151*
SIN/COS	Nonreal-Time	49	237*
Square Root	Real-Time	141	77 - 108
Square Root	Nonreal-Time	99	276

* Time to computer both sine and cosine of angle

In addition to sine/cosine, arc-tangent, arc-sine/arc-cosine, and square root subroutines contained in the two packages, the real-time package includes an executive program. By using an external real-time clock, this program will organize the routine and nonroutine activities of any processing system by maintaining a scheduling table. The executive program is divided into three sections:

- Schedule Routine - for controlling the order of execution of the various subroutines within the total processing system.

- Initiation Processor - for setting the initial condition necessary for the processing system. It sets index registers, clears memory registers if necessary, and initializes counters. This routine must be rewritten for each new processing system.

- Interrupt Processors - allow independent operation of subprograms by priority by automatic selection.

Utility Programs

The utility program package contains *ALERT* SNAP relocatable load, paper tape memory dump, and typewriter output routines. The relocatable load routine is used to load any SNAP assembled program. Paper tape memory dump is used to dump memory contents to paper tape in a format loadable by either *ALERT* bootstrap or SNAP relocatable loader. Four words per line of octal or instruction information may be typed from memory by executing the typewriter output routine.

Confidence Test Programs

Confidence testing includes diagnostic routines for memory, central processor, and peripheral devices. The diagnosis for each follows:

- Memory - malfunctions are located by a reading and writing exercise for each memory location in a series of test patterns. Failure of error causes the pattern being written, the memory address and the pattern read from the failure address to be displayed.

- Central Processor - tests exercise every instruction in the repertoire. Each test executes an order and evaluates the results for all possible cases. An error is specified by printout on the typewriter stating the failing instruction.

- Peripheral Devices - are required to generate or receive every character used during normal operation. Malfunction is detected by failure to generate or receive.

H-800/ ALERT SUPPORT SOFTWARE SYSTEM

The support package consists of two parts: H-800/*ALERT* simulator and H-800/*ALERT* symbolic notation assembly program (SNAP-8). The simulator program was written during the initial phase of computer development. It simulated the execution of all *ALERT* instructions on the Honeywell 800 commercial scientific computer. Although very useful, the simulator requires machine language coding of instructions. SNAP-8 was written to make the conversion.

INSTRUCTION REPERTOIRE

ALERT offers an instruction repertoire adequate for the most complex situation. The following list includes mnemonic, its definition, execution time in microseconds, and comments concerning the execution. The word format is described in the technical description, page 12, and will clarify the following notes to the programmer.

NOTES

Indexing and Indirect Addressing operations are specified in the address variant portion of the instruction. All address instructions may use indirect addressing and may be indexed except those working explicitly with the index register contents. These are designated in the list as not indexable. Since the address variant in an indirect address has the same meaning as in the original instruction word, indirect addressing may be continuous and indexing, if desired, will be performed at the last indirect address recursion. Computer register contents remain unchanged unless change is explictly stated.

Indexing and indirect addressing consumes one additional microsecond of execution time each.

The overflow indicator stores the two's complement overflow of the accumulator. It is cleared by testing.

The carry indicator stores the true binary carry-out of the high-order or sign. Carry is never cleared and always contains the result of the last accumulator arithmetic operation.

ABBREVIATIONS

Customary abbreviations used in the list follow.

( ) - "The contents of"

A - The Accumulator

B - The B Register

X, Y - The address of the memory location(s) referenced by this order; the address field of the instruction

XR_n - The Index Register referenced by this order (n = 1 to 6)

SR - Sequence Register

→ - "Replaces"

INSTRUCTIONS

The entire instruction list for *ALERT* is presented on the following pages.

Mnemonic		Exec. Time (μsec)	Comments
ADD	Add to Accumulator	2	(A)+(X)→A; the arithmetic is two's complement binary. Sense Overflow and Carry (ie, turn on Overflow or Carry function if either occurs).
ADM	Add to Memory	7	(A) + (X) → X; Overflow and Carry are not altered.
AIX	Augment Index Immediate	3	NOT INDEXABLE, NOT INDIRECTABLE: $(XR_n)+X \rightarrow XR_n$. This is an "immediate" form of AUX. The 15 bits of (XR_n) are added to a word composed of the address field of this order in the low-order 15 bits.
AUX	Augment Index	3	NOT INDEXABLE: (XR_n) + (X) → XR_n. Note that this is an absolute add of two 15-bit quantities.
BAR	Branch and Return	6	Store (SR) in X, and then change SR to X+1. The (SR) stored in X shall be the address of the next instruction following the "BAR".
DJX	Decrement and Jump on Index not Zero	2	NOT INDEXABLE: $(XR_n) - 1 \rightarrow XR_n$; change SR to X if $(XR_n) \neq 0$.
DLD	Double-precision Load	3	(X) → A, (X +1) → B.
DST	Double-precision	10	(A) → X, (B) → X + 1.
EXC	Execute	1	Execute the instruction at location X. Then, take the next instruction from the location specified by the SR. Note that this order is only able to execute one-word instructions. It is as if the instruction to be executed were taken from the location of the EXC itself.
EXT	Extract	2	(A) · (X) A ("·" = logical AND)
HAD	Half ADD	2	(A)$\oplus$(X) A ("$\oplus$" = exclusive OR)
JAN	Jump on Accumulator Negative	2	Change SR to X if (A) < 0. Overflow and Carry are ignored.

Mnemonic		Exec. Time (μsec)	Comments
JAP	Jump on Accumulator positive	2	Change SR to X if (A) > 0. Overflow and Carry are ignored.
JAZ	Jump on Accumulator Zero	2	Change SR to X if (A) = 0. Overflow and Carry are ignored.
JIX	Jump on Index not Zero	2	NOT INDEXABLE: Change SR to X if $(XR_n) \neq 0$.
JMP	Jump	2	Change SR to X.
LDA	Load Accumulator	2	(X) → A.
LDB	Load B Register	2	(X) → B.
LDX	Load Index Register	2	NOT INDEXABLE: (X) → XR_n.
LIM	Load Interrupt Mask	2	(X) → Interrupt Mask Register.
RSS	Restore Status V = 0	2	Set the following CP status functions equal to the bits of X, as follows (bit 0 = low order): Unused bits should be 0's in the H-387.

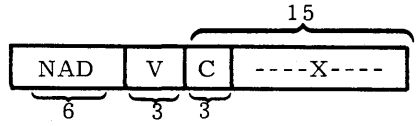
SET	to equal bit:
Overflow	6
Carry	7
Expon. Overflow	8
Expon. Underflow	9
Div. Overcapacity	10
Interrupt Block	11

NOTE

The action on the interrupt block is delayed until the next instruction is fetched.

(NAD) No Address Orders

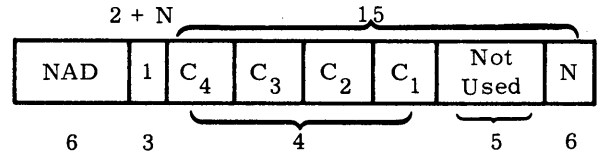
These orders share a common operation code, and use the address field to define the specific operation, as shown below.



General form of the NAD order.

V = 0 C = 0	Pass (PAS)	2	No operation. Go to the next instruction in sequence.

Mnemonic		Exec. Time (μsec)	Comments
V = 1	Shift (SFT)	2 + N	



Shift (A), or, in the case of double-precision, shift the contents of A and B taken together as a 48-bit register, by N bits, as follows:

C_1 0 = single precision
1 = double precision

C_2 0 = left shift
1 = right shift

C_3 0 = rotate, or "end-around"
1 = arithmetic

C_4 0 = interpret C_2, C_3, C_4 only
1 = hop sign of "B" IFF C_3 = 1 and C_4 = 1

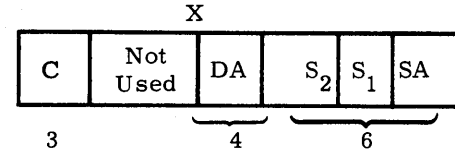
Notes:

1. In a "rotate", the low-order and high-order bits are considered to be adjacent.

2. In an arithmetic, shift, a right shift duplicates the sign in the emptied positions, and a left shift fills with binary zeros.

V = 2 Alter register (ALR X) 2

Alter the control registers according to the bits of X, as follows:

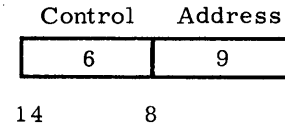


Transfer the register designated by SA to the register designated by DA, or exchange SA and DA.

SA = Source Address

Mnemonic		Exec. Time (μsec)	Comments
			$\frac{S_2 S_1}{0\ 0}$ = Straight Transfer 0 1 = Transfer negative (two's complement) 1 0 = Transfer absolute value DA = Destination Address C — Description 000 One-way transfer within CP 001 Exchange transfer within 01- One-way transfer with source located in RWC 10, 11- Reserved for future expansion of I/O capability The foregoing are limited to the following combinations: (B) → A (A) → B (A) ⟷ (B) (XR_n) → A (A) → XR_n - (A) → A |(A)| → A (RWC Current Address) → A
V = 3	Skip if signal is not set (SKN	3	Skip the next instruction if one of the 15 internal test points specified by the 15 bits of X is not set. X 14---------- 0 When more than one point is tested, skip if all are not set.

Mnemonic		Exec. Time (μsec)	Comments
			The points tested are as follows:
			Bit — Test Point
			0-5 Console Sense Switches 6-1
			6 Arithmetic Overflow
			7 Arithmetic Carry
			8 FP Exponential Overflow
			9 FP Exponentail Underflow
			10 Division Overcapacity
			12 Emergency External Interrupt
			11 Interrupt Block
			13-14 Not used
	Note: Note that the Overflow, Underflow, Overcapacity and Emergency Interrupt Points (6, 9, 10, 11, 12) are cleared when tested by this order.		
V = 4	Control and Skip (SKC)	4	This instruction transmits questions or commands to devices attached to the basic I/O bus. If a specific "yes" response or acknowledgment is not received, the next instruction in sequence is skipped. The 15 bits of X are divided as follows:



The address selects one of a possible 512 external devices. The Control portion transmits the following questions or commands:

Did the device interrupt?

Is this device busy?

Did this device have an error?

Start this device.

Stop this device.

Mnemonic		Exec. Time (μsec)	Comments
V = 5	Set External Point (STE)	2	Send a signal to one or more of the the up to 15 external test points signified by the 15 bits of X is not set. When more than one point is tested, skip if all are not set.
V = 6	Skip if External (SKE) Signal is not set	3	Skip the next instruction if one of the up to 15 external test points signified by the 15 bits of X is not set. When more than one point is tested, skip if all are not set.
V = 7 C = 0	Halt (HLT)	2 + Δ	Halt the execution of CPU instructions: Notes: 1. Peripheral Transfers in progress through the buffered I/O are not halted, but proceed to completion. 2. When the machine is halted, interrupts will still be honored, and the machine restarted via the sub sequence. The sequence at the moment of sub-sequence is set at the address of the halt instruction. 3. The machine may be restarted at the next instruction in sequence by manually depressing the continue button on the operator's panel.
V = 7	Set/Reset Block (SRB)	2	This instruction changes the state of the interrupt block according to the least significant bit. If $X_0 = 1$, set the interrupt block. If $X_0 = 0$, reset the interrupt block. All other bit positions are to be 0's.
PIN	Peripheral Input and Skip	8 if skip 4 if no skip	Store the 24-bit quantity on the input bus in X, if the bus is ready, and skip the next instruction in sequence. If the bus is not ready, do not disturb (X), and execute the next instruction in sequence.

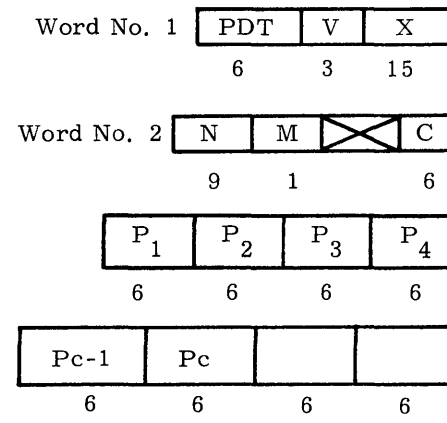
Mnemonic		Exec. Time (μ sec)	Comments
POT	Peripheral Output and Skip	4	Transfer the 24-bit quantity in X to the output bus, if the bus is ready, and skip the next instruction in sequence. If the bus is not ready, do not transfer (X) to the output bus, and execute the next instruction in sequence.
SKM	Skip if Accumulator and Memory are equal	4	Skip the next instruction if (A) = (X)
SKX	Skip on Index High	4	NOT INDEXABLE: Skip the next instruction if $(XR_n) > (X)$. Note that this is an absolute 15-bit comparison of (XR_n) with (X).
SMP	Superimpose	2	(A) v (X) → A ("v" = logical OR).
SMZ	Skip if Memory is Zero	3	Skip the next instruction if (X) = 0.
SST	Substitute	7	Using (B) as a mask, substitute (A) into X, protecting the old contents of X. In Boolean form: $(A) \cdot (B) \vee (X) \cdot (\overline{B}) \rightarrow X$
STA	Store Accumulator	6	(A) → X.
STB	Store B Register	6	(B) → X.
STI	Store Interrupt Register	6	Contents of Interrupt Register → X.
STX	Store Index Register	6	NOT INDEXABLE. $(XR_n) \rightarrow X$.
STS	Store Status	7	Transfer the following CP status functions to location X, protecting the high-order 12 bits of X. All these functions are set to zero after transfer. Bit positions 0 → 5 and 12 → 14 should be 0's.

Transfer the following function:	To this bit position of X:
Overflow	6
Carry	7
Expon. Overflow	8
Expon. Underflow	9
Div. Overcapacity	10
Block History	11

Mnemonic		Exec. Time (μsec)	Comments
SUB	Subtract from Accumulator	2	(A) - (X) → A. Sense Overflow and Carry.
SXI	Skip Immediate on Index High	3	NOT INDEXABLE: Skip the next instruction if $(XR_n) > X$. This is an immediate address form of SKX. In this instruction. the 15-bit (XR_n) are compared to a word composed of the address field of this order in the low order 15 bits, and 9 high-order zeros.
TLY	Tally	7	(X) + 1 → X.
XML	Exchange Interrupt Mask	6	The contents of the Interrupt Mask Register are exchanged with (X).
MPY	Multiply	12	(A) x (X) → AB. In the product, the sign of "B" is made equal to the sign of "A". Overflow can occur only in one case, when the largest negative number is multiplied by itself. In this case, the overflow indicator is set (the same one used for add and subtract), and $A = (40000000)_8$ and $B = (40000000)_8$.
DIV	Divide	30	$\frac{(AB)}{(X)}$ → A. Remainder → B. In the computation, the sign bit of B is discarded and the sign of the dividend is the sign of (A). The following relationships between operands and results specify the divide procedure. 1. DIVIDEND = (QUOTIENT X DIVISOR) + REMAINDER 2. $\lvert$REMAINDER$\rvert$ < $\lvert$DIVISOR$\rvert$ 3. The remainder is a two's complement number with the same sign as the dividend (ie, the

Mnemonic		Exec. Time (μsec)	Comments
			sign of A) except when the remainder is zero and the dividend is negative. 4. Divide overcapacity DIVO will occur if either of the two following relationships are not met: $\|(AB)\| > \|(X)\|$ or $\|(AB)\| = \|(X)\|$ AND the dividend and the divisor have different signs. When DIVO occurs the original dividend is returned to the A B register when the sign of B made equal to the sign of A; and DIVO flip-flop in the CP is set.
LCH	Load Character	2	Take the specified 6-bit character from (X) and insert it in the corresponding position in the Accumulator, protecting the rest of the accumulator. The address variant has special meaning in this order: Hi-order bit - indirect address Two lo-order bits - signify which of the 4 characters is to be used: 01 = character number 1 10 = character number 2 11 = character number 3 00 = character number 4. Note that if indirect addressing is used, then the address variant of the indirect address word has the normal meaning.
SCH	Store Character	7	Take the specified 6-bit character from (A) and insert it in X, protecting the rest of (X). The address variant has special meaning as above.
CSK	Characters skip if equal	5	Skip the next instruction if the specified character in (A) equals the corresponding character in (X). The address variant has special meaning as above.

Mnemonic		Exec. Time (μsec)	Comments
PDT	Peripheral Data Transfer	$3 + \frac{29C}{4}$	T ansfer data across the buffered I/O bus to or from sequential locations starting with X, until an external end-of-record signal occurs, or N words are transferred, whichever comes first. In the case when N = 0, transfer terminates an external signal only. This is a multi-word instruction, whose format is as follows:



enough additional words to contain "c" P-characters

The first word has the usual meanints. In the second word, N specifies the number of words in the record ($1 < N < 511$; N = 0 means "ignore the word count"), and c specifies the number of "P" characters. M=0 specifies the unpacked mode. M = 1 specifies the 6-bit packed mode. The "P" characters are identical to the "V" characters in the H-200 PDT order (the "Interlock bit" of P_1 has no meaning).

PCB	Peripheral Control	$3 + \frac{29C}{4}$ max	Change SR to X if the answer to the question asked by the "P" characters is yes, or if the command cannot be executed. Format of this order is the same as for PDT, except that "M" and "N" are unnecessary. Again, the "P" characters are identical to the "V" characters in the H-200 PCB order.

SYSTEM SUPPORT EQUIPMENT

ALERT is supported by a complete complement of system support equipment. Included are:

- Ground Test and Maintenance, consisting of:

  Computer Test Unit

    Operator Control Unit

    Tape Reader

    Power Supplies

  Memory Loader Unit

    Loader

    Tape Reader

    Memory Exerciser

    Power Supplies

- Peripheral Devices:

  Paper Tape Reader

  Paper Tape Punch

  Keyboard Printer

For further information request "System Support Equipment", Document Number FL-765-R1.

For more detailed information...

CONTACT YOUR NEAREST HONEYWELL REPRESENTATIVE

or write directly to: Honeywell Inc., Marketing Department,
13350 U. S. Highway 19, St. Petersburg, Florida
Phone 525-1121

FL-665-R1A